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ECE

PM 1 - B

ACE Academy

Electronic Devices & Circuits

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* Standard Values:

$\Rightarrow$ $n_i = 1.5 \times 10^{10}$ cm^{-3} $\rightarrow$ Si] AT 300°K.

$= 2.5 \times 10^{13}$ cm^{-3} $\rightarrow$ Ge]

$\Rightarrow$ E_G (ev)

		0°K	300°K
Ge	:	0.785	0.72
Si	:	1.21	1.1

$\Rightarrow$ $\mu_n = 3800$ $cm^2/v\text{-}sec$] Ge] AT 300°K

$\mu_p = 1800$ "

$\mu_n = 1300$ "] Si

$\mu_p = 500$ "

$\Rightarrow$ $q = 1.6 \times 10^{-19}$ C.

$c = 3 \times 10^{8}$ m/sec.

$k = 8.62 \times 10^{-5}$ ev/°K.

$T = 27°C$ (OR) 300°K (default).

* Reference Text-Books:

① Integrated Electronics by Millman and Halkyins.

② Solid State Devices by Streetman.

* Law of Preparation:

⇒ "All technical and Non-technical (Maths, English, General ability, Numerical ability) are to be prepared for Gate examination it required vary preparation time depending on complexity of subject."

* Topics:

(I): Semiconductors.

(II): Diodes.

(III): Transistors & opto electronics

(IV): VLSI.

☆ Intrinsic (or) Pure Semiconductors:

→ Most of the electronic devices are made up of either silicon (Si) (or) Germenium (Ge) with the following Configuration:

$$Si\,(14) \longrightarrow 1s^2\,2s^2\,2p^6\,3s^2\,3p^2.$$

$$Ge\,(32) \longrightarrow 1s^2\,2s^2\,2p^6\,3s^2\,3p^6\,3d^{10}\,4s^2\,4p^2.$$

⇒ If two silicon atoms 1 & 2 are brought very closed to each other then atom-1 expects valance shell $4e^-$ of atom-2 to be given atom-1. so that incomming $4e^-$ and existing $4e^-$ make atom-1 to have $8e^-$ in valance shell thay gets saturation and stability.

$$\Rightarrow \quad Na\,(11)^{+} \xrightarrow{\quad 1e^- \quad} Cl^-\,(17)$$

$$1s^2\,2s^2\,2p^6\,3s^1 \qquad\qquad 1s^2\,2s^2\,2p^6\,3s^2\,3p^6 + 1e^-$$

→ If Sodium and Clorine atom are brought close to each other then Sodium will give away $3s^1$ electrone to Clorine become +ve ion and gets Stability with $8e^-$ in Valance shell

(2^{nd} orbit). Clorine by accepting 1 electron becomes -ve ion and gets Stability with $8e^-$ in valance Shell (3^{rd} orbit). These two ions attract each other and ionic bond forms.

→ Clorine gets Stability by loosing $1e^-$ (or) by gaining $7e^-$. Hence, loosing versus gaining ratio is 1:7.

→ Silicon atom can gets stability by loosing $4e^-$ (or) by gaining $4e^-$. Hence loosing versus gaining ratio is 4:4 (or) 1:1. In the case of sodium and Clorine since ratio is non-uniform exchange will occur. In the case silicon since ratio is uniform sharing of electron will occur. After sharing gets completed a 3-D crystal lattice gets created.

⇒ Fig. (1) Shows a 2-D view of crystal lattice of silicon.

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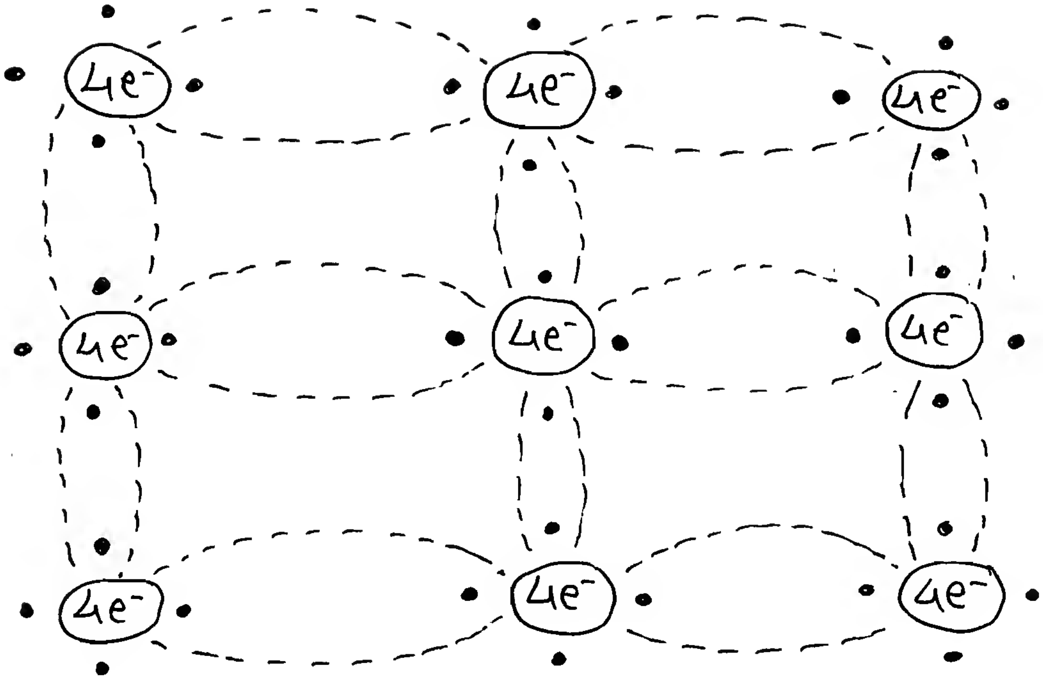

Fig-① Crystal lattice

⇒ Fig-② Shows normal atomic model of a silicon atom.

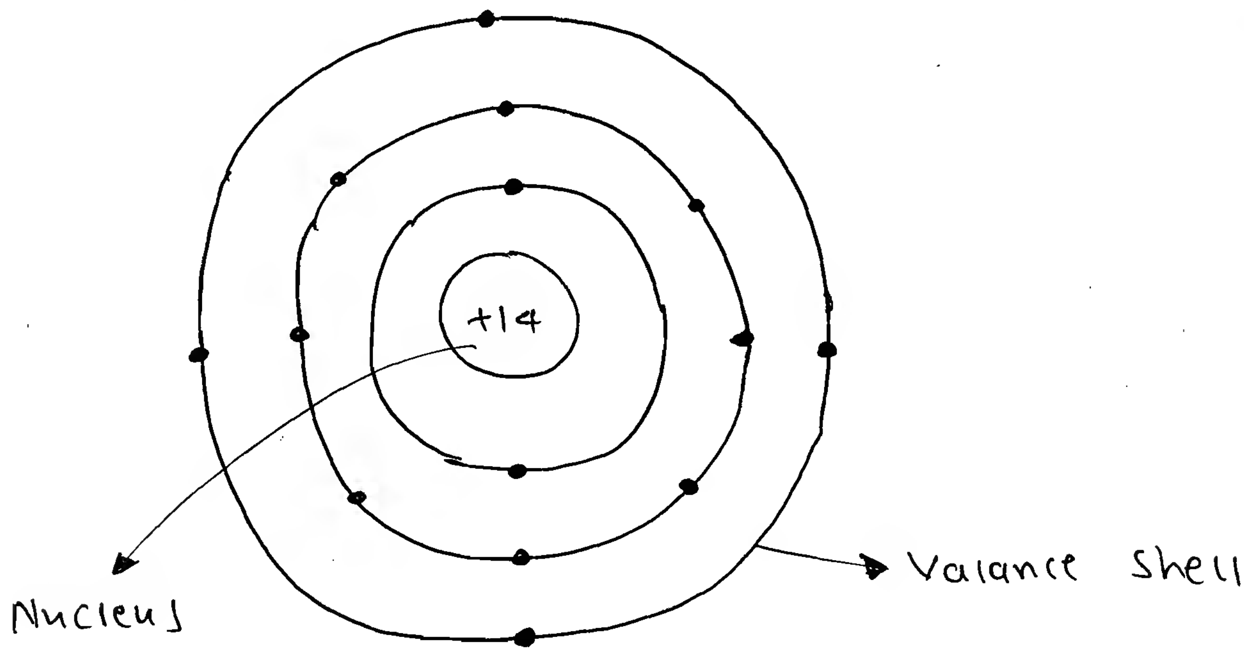

Fig-② - Atomic model of silicon atom.

⇒ All atoms are electrically nutral.
(No. of Proton = no. of electron).

⇒ If a charge carrier moves through a

unit cross sectional area then per unit it can produce current i.e.

$$I = \frac{dq}{dt}.$$

⇒ All the -vely charge electron bound to +vely charge nuclues. Such bound are immobile electron can not support current.

⇒ If an external force is applied to electron more than electric force applied by nucleus then electron comes out of force of attraction of nucleus becomes free. Such free electrons are mobbile electron can support current.

⇒ As we move from the nucleus force of attraction decreases. hence to comment on conductivity only valance shell electrons only to be considered as they can made free easy.

⇒ FIG - 3 shows modified atomic model representation of silicon atom.

⇒

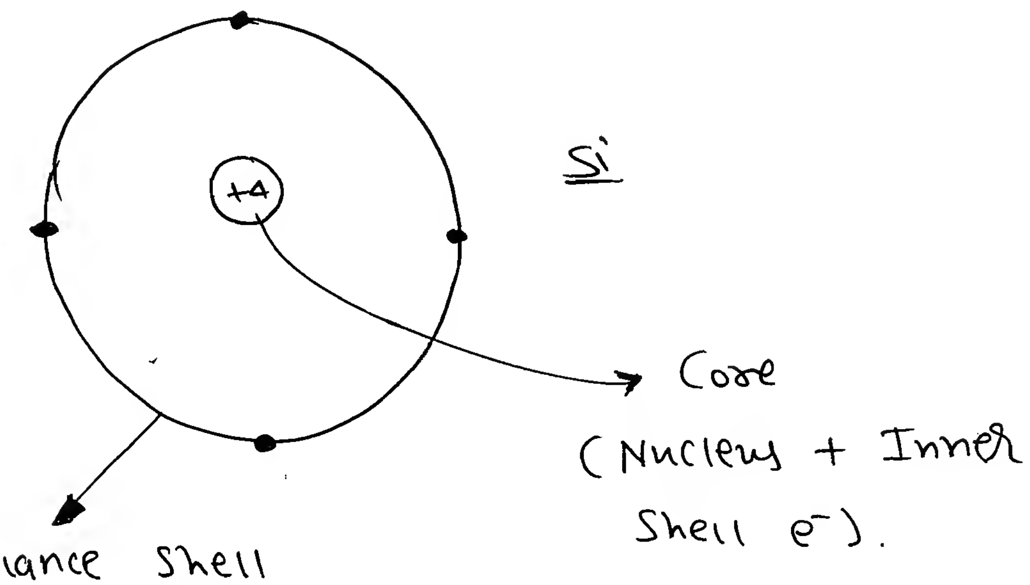

Fig-3 - Modified atomic model of si.

→ Fig-③ is valid representation to comment on conductivity of silicon (or) Germenium (or) any atom of group 4 of periodic table. Using this a set of 5 atoms (or) Superimpose as in fig-④.

⇒

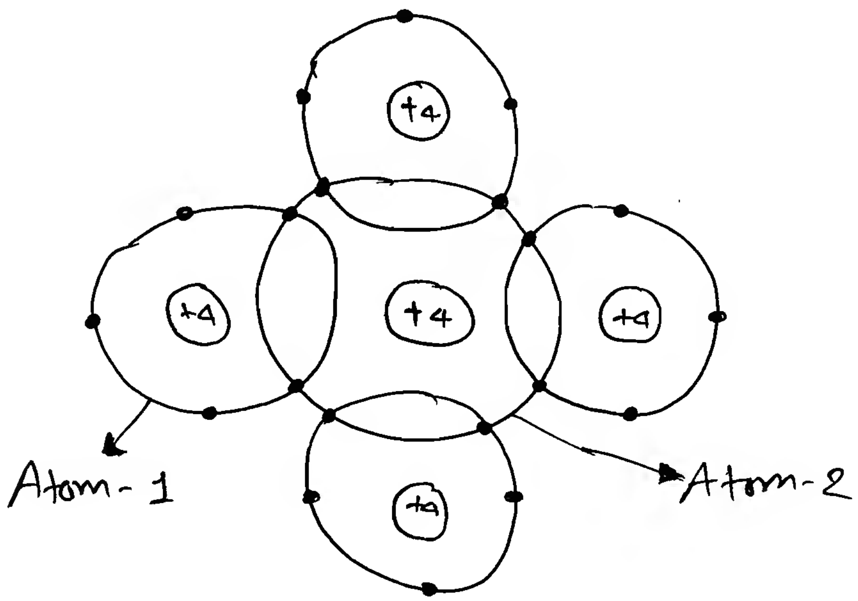

Fig-4

* Energy Band Diagram:

⇒ Collection of Closedy Spaced discrete energy level is called energy band diagram.

⇒

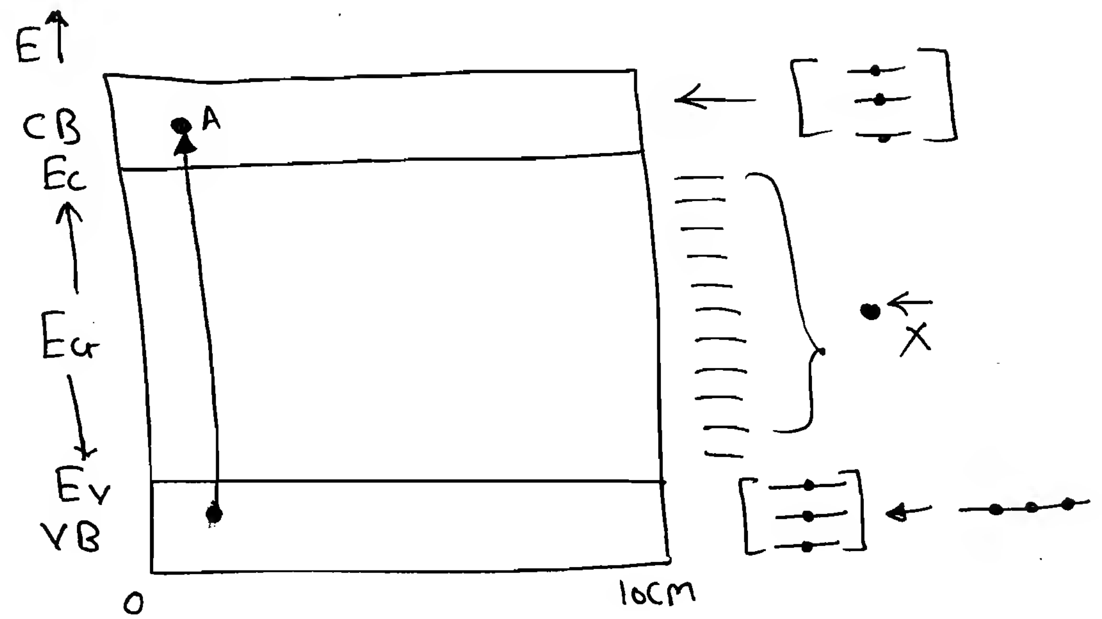

Fig- 5 - Energy Band diagram.

⇒ If all the atoms of a crystal are pulled seperately and kept at larger distance from each other then all the atom's valance shell electrons will occupy the same energy level.

⇒ If atoms are broughten very closed to each other to form a crystal then so many electrons sitting at the same energy violates Pauli's exclusion principle which states that no two electrons belonging to the same interacting

System can have the same value for the quantum numbers n, l, m & s.

⇒ To satisfy Pauli's principle electron diverges and form valance band (VB). An electron in VB (lower energy level) belongs to valance shell and it is bound hence can not support current.

⇒ If an external energy is applied to an e^- more than the ~~electric~~ energy with which the nucleus pulls the electron, the electrons becomes free and gets aexicted move to higher energy and found conduction band (CB). An electrons in CB (higher energy level) is of ~~loose~~ type free and can support the current.

⇒ $\underline{\underline{E_c}}$: Lowest Energy Level (or) Edged of Conduction band.

⇒ $\underline{\underline{E_v}}$: Highest Energy Level (or) Edged of Valanced band.

⇒ Between E_c & E_v, energy level exist but in them electrons do not exist and it is called forbidden band (or) Energy band gap. i.e. E_g

⇒ $$\boxed{E_{g\,(eV)} = E_c - E_v}$$

⇒ As E_g increases material becomes insulator, As E_g decreases material becomes Conductor.

⇒ E_g approximately zero for Conductor.

⇒ At 0°K, all valance shell electrons are bound in covelent bond (i.e. bound to parent nuclie). Hence, material acts as insullator.

⇒ Covelent bonds are force, existing but not visible. Hence shown by dotted line.

⇒ At 300 K, an electron breaks a covelent bond (i.e. comes out of force of attraction of nucleus) becames free and can be drifted to produce electron drift current In and make material Conductor.

* e^- Current (I_n)	Hole current (I_p).
① A free electron is moving.	① An electron is moving from one bound state to other.
② An electron is moving in conduction band.	② An electron is moving in valance band.
③ An electron is moving at higher energy level.	③ An electron is moving at ~~higher~~ Lower energy level.
④ An electron is moving through interatomic gap.	④ An electron is moving from one covelent bond to other.

⇒ Non-existance of electron in a covelent bond is defined as space.

⇒ To under-stand, the current given by space a set of 8 atoms (or) superimpose as shown in fig-6.

⇒ Using atomic model representation of fig-③, ABCDE are covelent bonds. Each dots is a valance shell electrons sitting in a covelent bond.

⇒ Fig-⑥ is atomic model representation of crystal lattice at 0°K.

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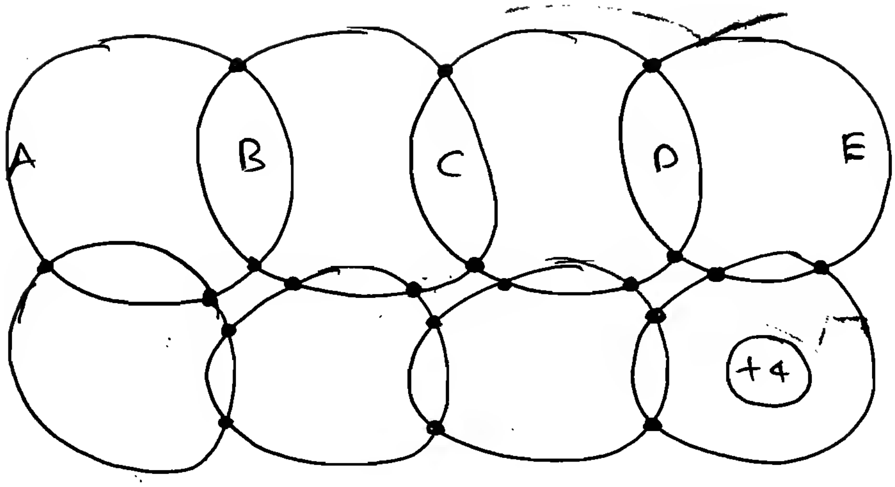


Fig - 6

⇒ At 300°K an electron breaks a covelent bond becomes free and creates space as shown in fig - 7.

⇒

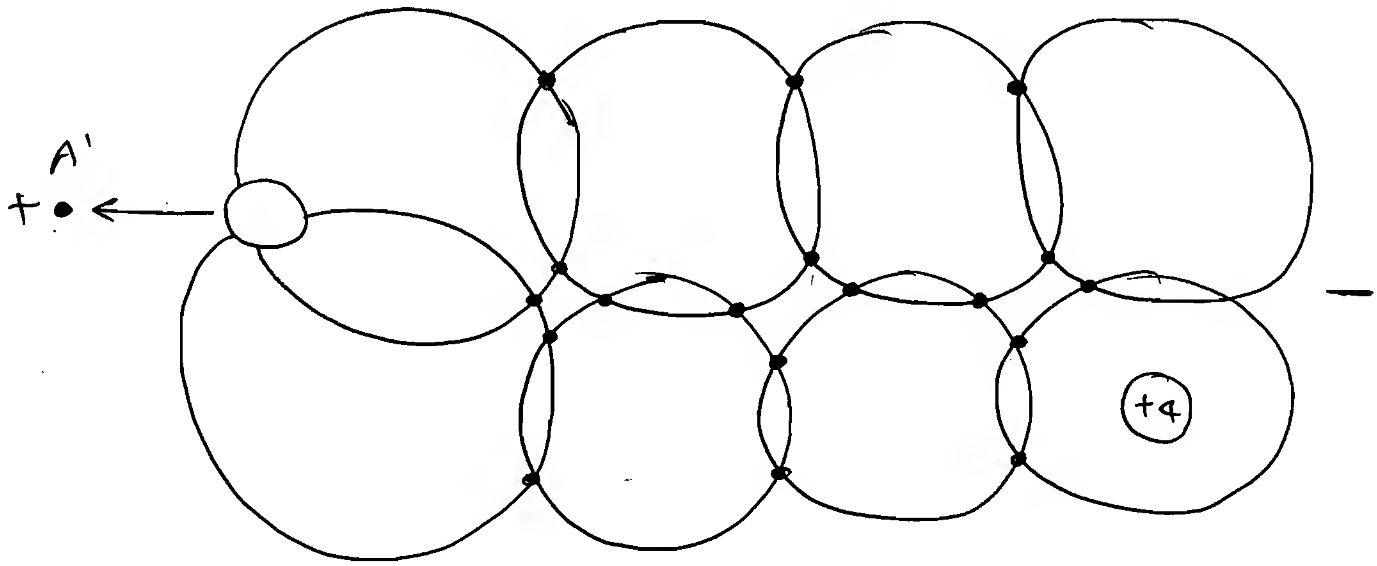


Fig - 7

→ An electron is drifting from E to A (Right to left) through EDCBA path. from EDCBA and producting current to right side as in Fig - 8.

⇒

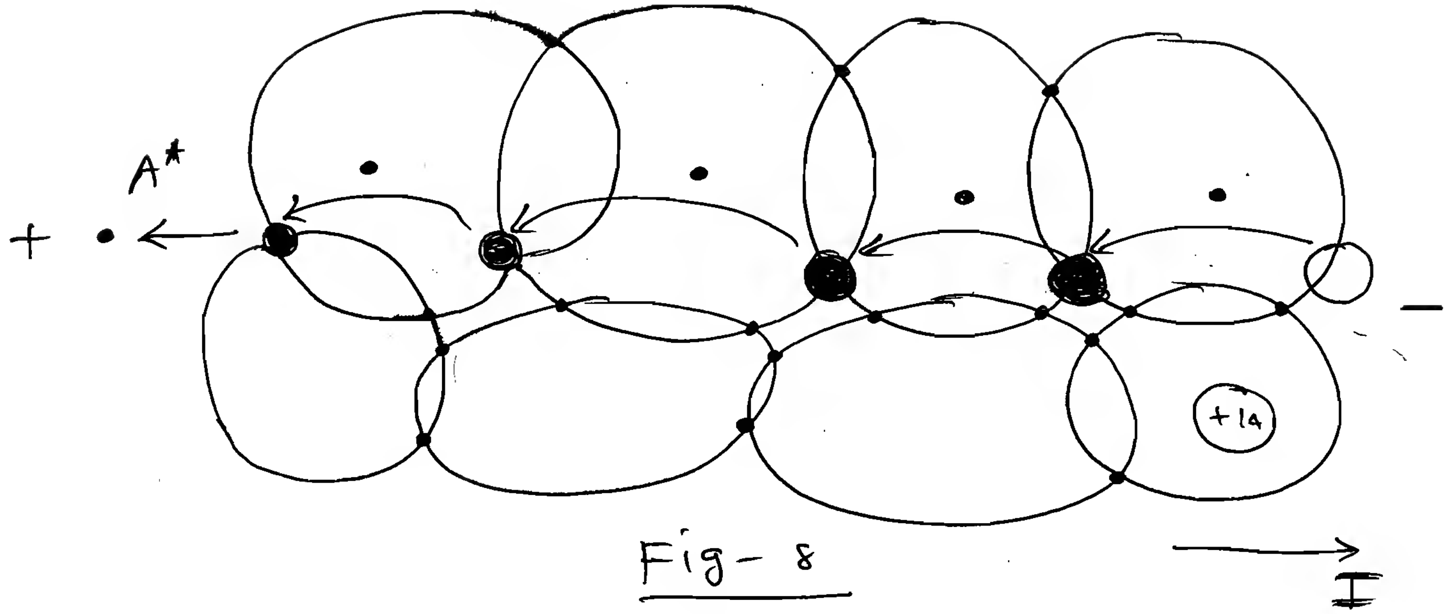


Fig- 8

⇒ The electron transition shown in atomic model of fig-8 are transfer to energy diagram as in fig-9.

⇒

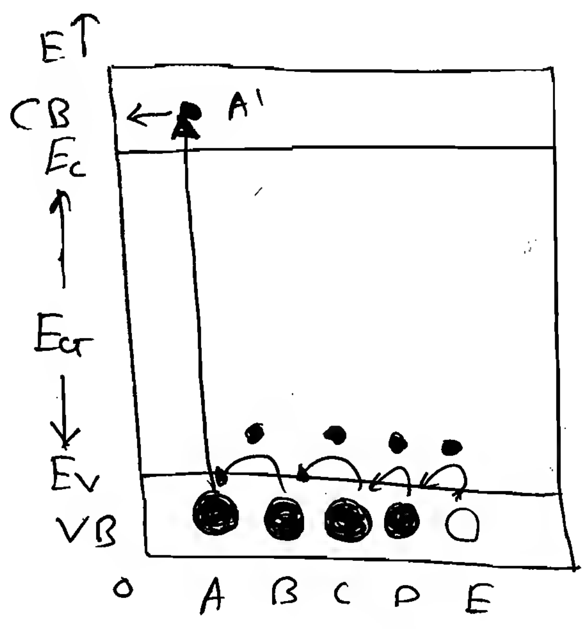


Fig- 9

⇒ Space motion from A to E through ABCDE path is producing current to right side. Hence space is defined as a +vely charged mobille partical called Hole.

⇒ If one electron goes to conduction band it leaves one hole in valance band hence called electron- hole pair (EHP) generation.

⇒ In n- intrinsic conduction,

$$\boxed{\Rightarrow \text{Free electron Concentration } n = \text{Hole consentration } p}$$

⇒ But electron current $\boxed{I_n > I_p}$ because mobility of electron μ_n is greater than mobility of hole μ_p (i.e $\boxed{\mu_n > \mu_p}$) and net current is sum of electron and hole currents.

i.e. $\boxed{I = I_n + I_p.}$

⇒ Drift current,

$$\boxed{I = \underbrace{nq\mu_n EA}_{I_n} + \underbrace{pq\mu_p EA}_{I_p}.}$$

$\therefore \quad I = I_n + I_p.$

$$\therefore \boxed{I = nqEA[\mu_n + \mu_p].}$$

⇒ Electrons and holes are moving opposite direction but current given by them will be in the same direction.

<u>Note:</u>

→ For IES exam (or) Engineering college teaching don't use fig - ③, ④, ⑥, ⑧.

☆ **Extrinsic (or) Impure Semiconductors:**

⇒ $\sigma = nq\mu_n + pq\mu_p$.

$R = \left[\frac{L}{\sigma A}\right]$.

$I = V/R$.

⇒ ✗ INT : 1mA (300°K) ⟶ 10mA (400 K) 127°C.

✓ INT : $\xrightarrow{\text{Impurities}}$ EXT.

1mA : ⟵ 300°K : ⟶ 10mA.

⇒ Without extrinsic semiconductor it is not possible to produce required current at room temp. and it is not possible to design an electronic device.

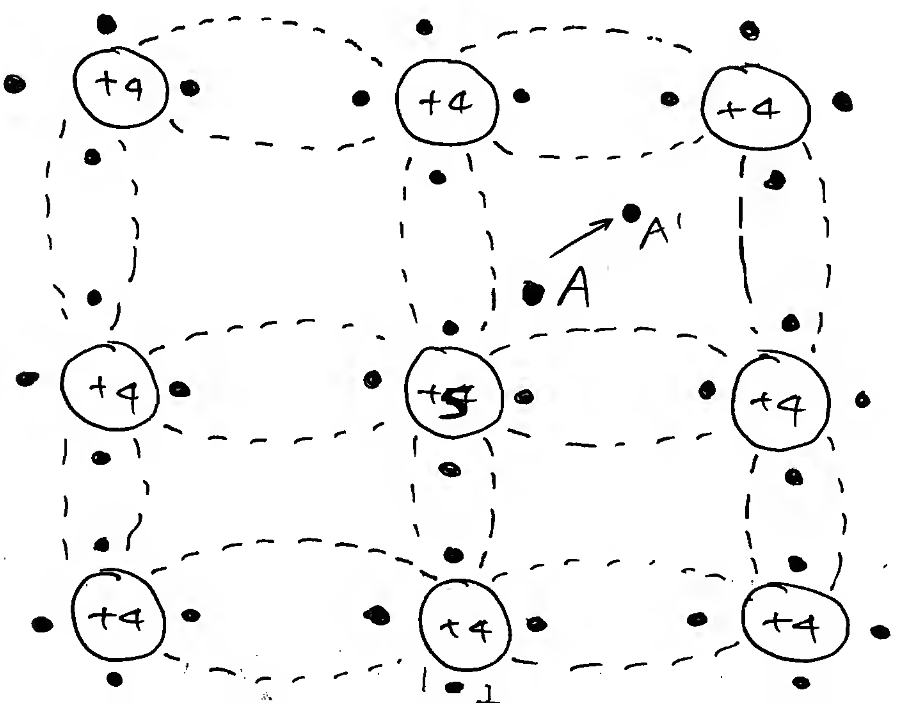
* **Extrinsic Negative type (or) Extrinsic n-Type. Semiconductor**

⇒ Penta Valent impurities (Fig - 2) like Phosphrus, Arsenic, Antimony (or) Bismuth are added to an intrinsic semiconductor.

⇒ When a pentavalent atom replaces, a tetravalent silicon (or) Germenium atom then out of five valance electron four electrons are supplied to four covelent bonds and one electron is excess as in crystal lattice (Fig - 1).

⇒ All such excess electron occupy a new energy level E_d at $0°K$ slightly below conduction band at 0.01ev for Germenium and 0.05 ev for silicon as in energy diagram (fig - 3).

⇒ Fig - 1 Fig -



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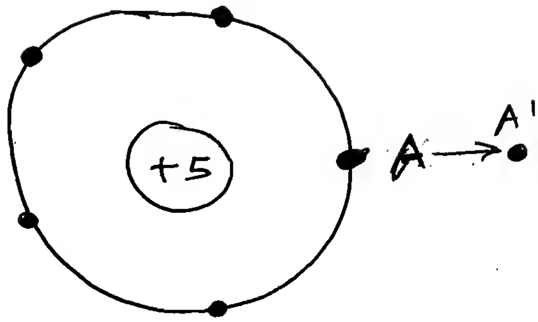

FIG - 2

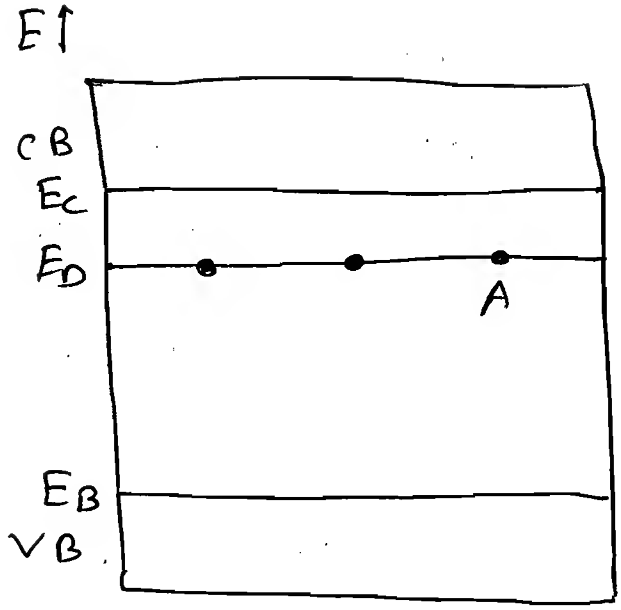

FIG - ③

⇒ At 0° K all intrinsic and extrinsic Semiconductors act as insulators.

⇒ At 0° K from Fig-3, $n = 0$ & $p = 0$ hence $\sigma = 0$, $R = \infty$ & $I = 0$. i.e. Insulators.

⇒

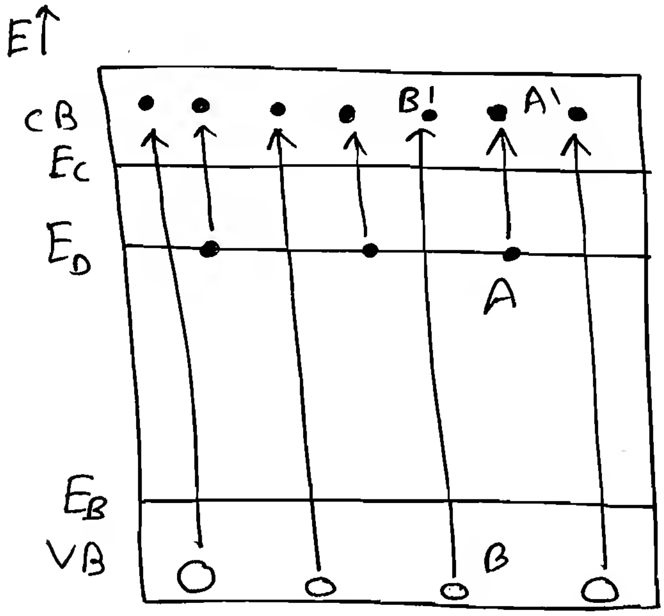

FIG - 4

⇒ At 50° K for Ge and 100° K for silicon pentavalent impurities loose excess electrons

becomes +ve ion called impurity ionization (I.I). Hence $n > 0$ and $p \cong 0$ ($p = 0$). Hence, $\sigma > 0$, $R < \infty$ and $I > 0$ i.e conductor.

⇒ Pentavalent atom is giving 1 e^- for support of current hence called donor atom.

⇒ E_D : donor energy level.

⇒ At 300° K electron hole pair (EHP) generation (OR) Band to Band (B.B) transition occurs. hence, n increases and p increases. Hence, σ increases, R decreases and I increases. i.e. more current is possible in extrinsic than intrinsic due to I.I. (Impurity Ionization)

⇒

$$\boxed{I = \underbrace{I_n(I.I) + I_n(B.B)}_{I_n} + \underbrace{I_p(B.B)}_{I_p} = I_n + I_p}$$

→ $I_n(I.I)$: Current due to electrons given by I.I.
  ↓ A'

→ $I_n(B.B)$: Current due to electrons given by B.B
  ↓ B'

→ $I_p(B.B)$: Current due to holes given by B.B
  ↓ B

⇒ Lightly bond electron becoming free can not create hole. A hole is created when electron breaks a covelent bonds.

⇒ To comment on the type of semiconductor never compare currents always compare concentration i.e.

$n = p$	$\longrightarrow$	INT.
$n \neq p$	$\longrightarrow$	EXT.
$n > p$	$\longrightarrow$	N - TYPE.
$n < p$	$\longrightarrow$	P - TYPE.

⇒ All intrinsic and extrinsic semiconductor are electrically nutral.

⇒ Charge carriers which are more in no. are called majority carriers and current given by them is called majority current i.e.

Majority carriers	$\longrightarrow$	e^-
Minority carriers	$\longrightarrow$	Hole
Majority currents	$\longrightarrow$	I_n
Minority currents	$\longrightarrow$	I_p

⇒ Negetively Charge electrons are majority Carriers. Hence, called extrinsic negative type Semiconductor.

* <u>Extrinsic Positive type (or) Extrinsic P-type (or) P-type Semiconductor:</u>

⇒ Trivalent impurities (Fig- ⑥) like Boron, Aluminium, Gallium (or) Indium are added to an intrinsic semiconductor.

⇒ When a trivalent atom replaces a tetravalent silicon (or) Ge atom then to four covelent bond only 3 valence e^- are supplied hence one excess hole created as in crystal lattice (fig-5). All such excees holes occupie a new energy level E_A at 0°K above valence band at 0.01ev for Ge and 0.05 ev for si. as shown in Energy diagram (Fig-7).

⇒

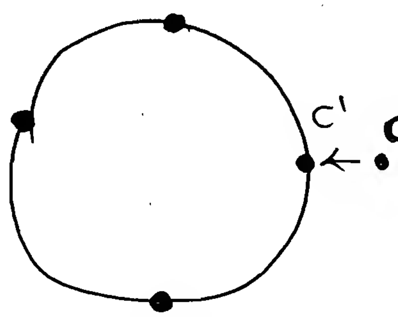

FIG- ⑥

⇒

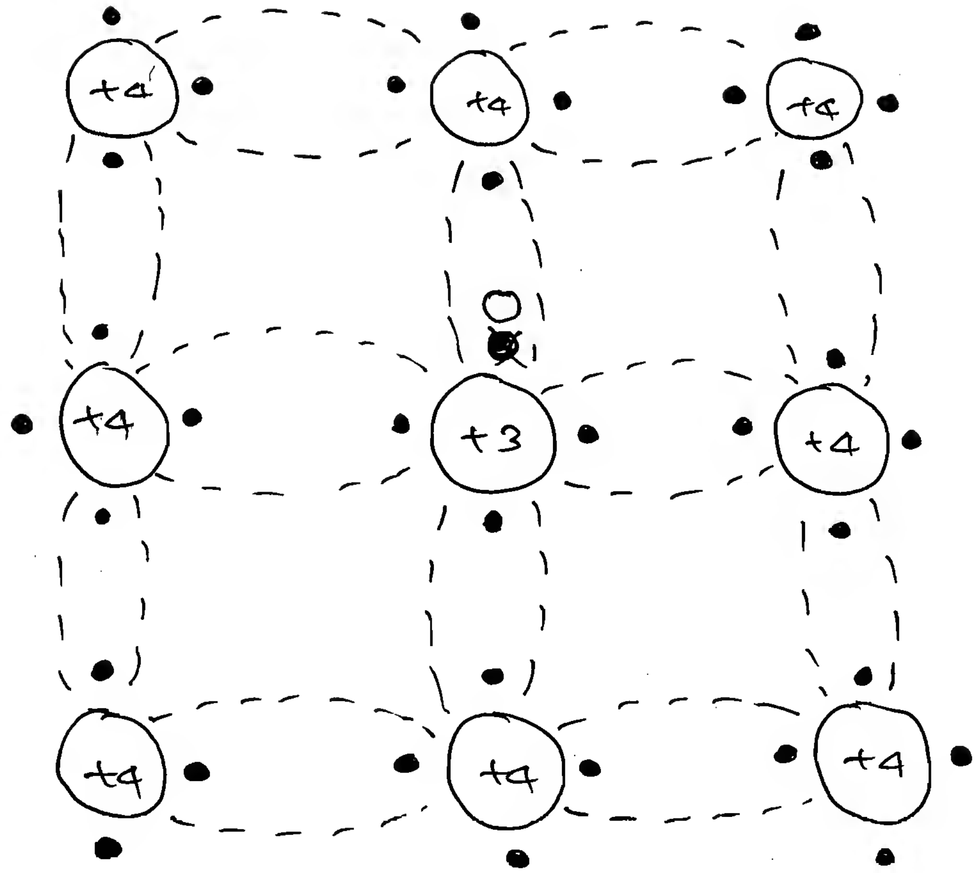

FIG - 5

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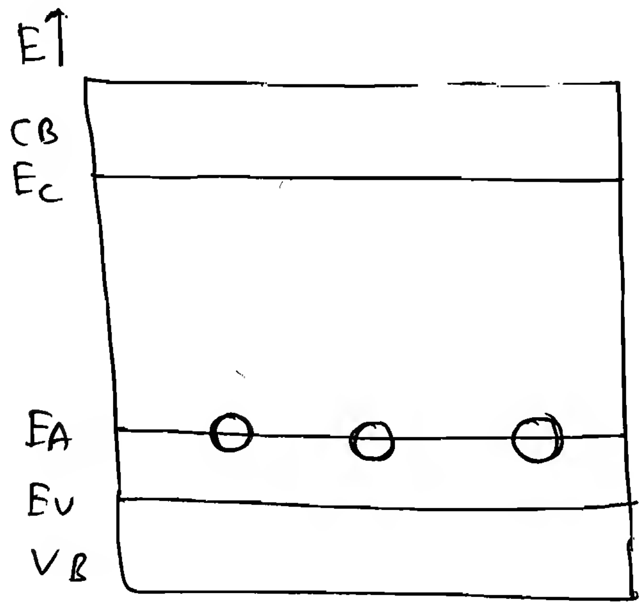


FIG - 7

⇒ At 0°K from fig-7 $n=0$ & $p=0$. Hence $\sigma=0$, $R=\infty$ & $I=0$. i.e. Insulator.

⇒ At 50°K for Ge (or) 100°K for Si electrons gain energy and move to holes at E_A level than all the

⇒

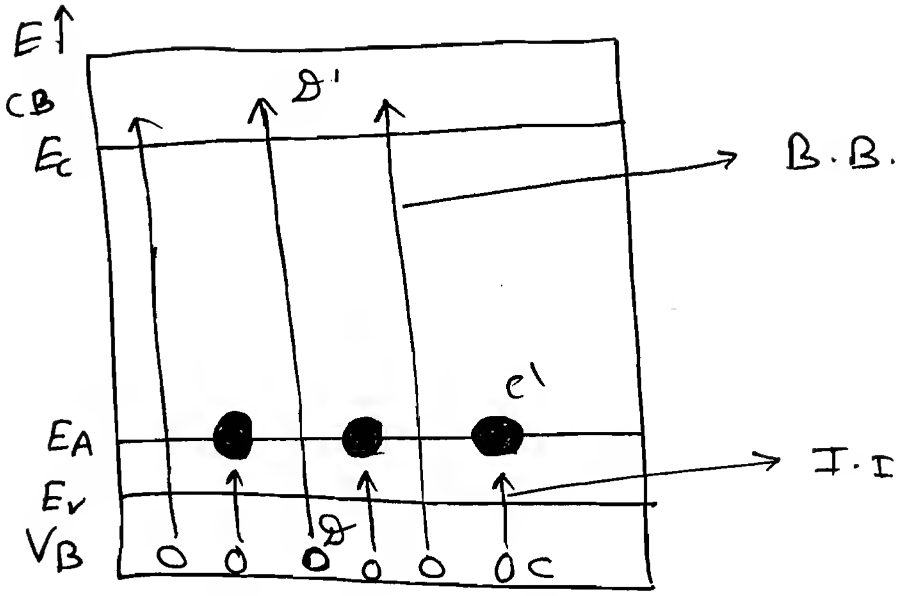


FIG - 8

holes at E_A level disappear and equal no. of holes get created in valance Band. Hence, $n = 0$ & $p > 0$. Hence $\sigma > 0$ $R < \infty$ & $I > 0$. i.e. Conductor.

⇒ Trivalent impurity by accepting electron becomes negative ion called impurity ionization (I.I). Trivalent atom by accepting e^- creates hole and supports current hence called acceptor atom.

→ E_A : Acceptor Energy Level.

⇒ At 300 K EHP Generation (or) Band to Band (B.B) transition occurs. Hence n increases and p increases hence σ increases R decreases and I increases.

⇒

Majority	Carriers	→	HOLE
minority	Carriers	→	e^-
majority	currents	→	I_p
minority	Currents	→	I_n.

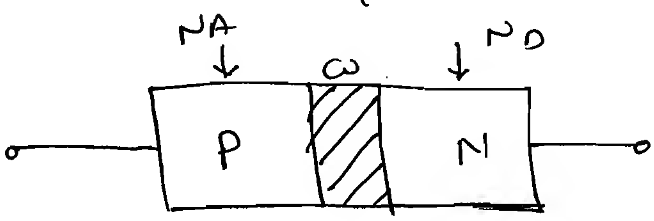
Note:

→ At very high temp. all extrinsic Semiconductors become intrinsic because band to band transition dominates (or) over through impurities ionization and at this temp. Usefullness of all electronic devices will get terminated.

⇒ **n-Type:**

	e^- (I.I)	e^- (B.B)	hole (B.B)	
300 k :	10^2	10^2	10^2	: $n \neq p \Rightarrow$ EXT.
400 k :	10^2	10^3	10^3	: $n \neq p \Rightarrow$ EXT.
700 k :	10^2	10^5	10^5	: $n \approx p \Rightarrow$ INT.

⇒



300 k : FB : + − : $W\downarrow \rightarrow I\uparrow$: ON

RB : − + : $W\uparrow \rightarrow I\downarrow$: OFF.

⇒ $\boxed{700^\circ K}$

(P) (N)

I	I

~~Switch~~

FB : + − : $\overrightarrow{IA}$

RB : − + : $\overleftarrow{IA}$

⇒ $\boxed{300^\circ K}$:

n	p	n

: Amplifier.

$\boxed{700^\circ K}$:

I	I	I

: Attenuator.

* Mass Action Law:

⇒ The Product of free electron and hole Concentration in an intrinsic (or) Extrinsic Semiconductor at a given temp. is a constant given by

$$\boxed{np = n_i^2} \quad \text{——— (1)}$$

Where; n_i : intrinsic Concentration given by

$$\boxed{n_i^2 = A_0 T^3 e^{-E_{G0}/kT}} \quad \text{——— (2)}$$

where A_0 is a constant dependent on

Semiconductor and independent on temp.

T : Temp in °K.

E_{G0} : Energy Band gap at 0°K.

k : Boltzman Constant in eV/°K.

⇒ $\boxed{300°K}$: INT : $np = n_i^2$

↓

N-type : $(n\uparrow)(P\downarrow) = n_i^2$

⇒ Consider an intrinsic Semiconductor at 300°K with $n.p = n_i^2$ say it is converted to n-type without changing temperature then n_i^2 is constant. Due to donor e^- concentration n increases hence prob. of hole recombine with electron increases. Increase to n and decreases to p counter make $n.p = n_i^2$ constant.

⇒ $\boxed{INT}$:

300°K : $n_1 P_1 = n_{i_1}^2$

400°K : $n_2 P_2 = n_{i_2}^2$.

⇒ Consider an intrinsic semiconductor at 300°K with $n_1 \cdot P_1 = n_{i_1}^2$ say temp.

increases to 400 K and $n_{i_1}^2$ to $n_{i_2}^2$.

Due to increase in temp. EHP generation increases hence n_1, P_1 increases to n_2, P_2 such that $n_2 \cdot P_2 = n_{i_2}^2$.

→ $n \cdot p = n_i^2$ is valid at a given temp.

If temp changes again valid hold for different value. i.e. $\boxed{n_1 \cdot P_1 \neq n_2 \cdot P_2}$

$$\Rightarrow \boxed{n_{i_1}^2 \neq n_{i_2}^2}$$

⇒ Based on electrical neutrality

$$\boxed{N_D + p = N_A + n} \quad \text{———} \quad (3)$$

⇒ LHS gives total +ve ~~ions~~ charges per cubic volume given by donor ions and holes.

⇒ RHS gives total -ve charges per cubic volume given by acceptor ions and electrons.

* <u>Case - I</u> :- <u>Intrinsic</u> (<u>$N_D = N_A = 0$</u>).

$$\Rightarrow \quad \cancel{N_D}^{\,0} + p = \cancel{N_A}^{\,0} + n.$$

$$\Rightarrow \boxed{n = p} \quad ✓ \quad \text{———} \quad (4).$$

From eq^n 1 & 4

$$\boxed{n = p = n_i} \quad \text{——— (5)}$$

Case - II : N - Type ($N_D > 0$, $N_A = 0$).

$\Rightarrow$ From eq^n - 3

$$N_D + \underbrace{\cancel{P_n}}_{\text{Neglect}} = \cancel{N_A}^{0} + n_n .$$

When, P_n, n_n is hole, free electron Concentration in N-Type.

$\rightarrow$ ~~N_D~~

$$\boxed{n_n \simeq N_D} \quad \text{——— (6)}$$

Note: $n.p = n_i^2$ is valid for only one Semiconductor which Can be Intrinsic (or) n-type (or) p-type. It is not applicable across multiple Semiconductors.

$$\rightarrow \quad n_n P_n = n_i^2$$

$$\rightarrow \quad \boxed{P_n = \frac{n_i^2}{n_n} \simeq \frac{n_i^2}{N_D}} \quad \text{——— (7)}$$

Case-III : P-Type ($N_D = 0,\ N_A > 0$).

$\Rightarrow$ $\cancel{N_D}^{0} + P_p = N_A + \cancel{n_p}$
neglect.

$\Rightarrow \boxed{P_p \simeq N_A}$ —— (8).

$\rightarrow$ $n_p P_p = n_i^2$

$\therefore \boxed{n_p = \frac{n_i^2}{P_p} = \frac{n_i^2}{N_A}}$ —— (9).

* Diffussion

$\Rightarrow$

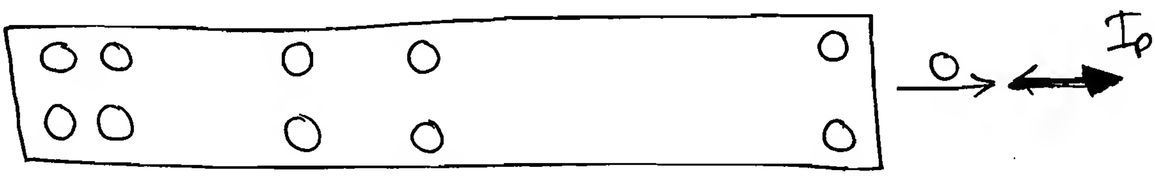


FIG-1.

$\Rightarrow$ Consider a P-type semiconductor as in Fig-1. Due to difference in concentration, holes diffuse from higher to lower (Left to right) concentrated area until uniform carrier concentration ($\frac{dP}{dx} = 0$) is achieved and produced hole diffussion current I_p where hole diffussion

Current density $J_p(x)$ is given by

$$\boxed{J_p(x) = \frac{I_p}{A} = -qD_p \frac{dp}{dx}.}$$

$\Rightarrow$

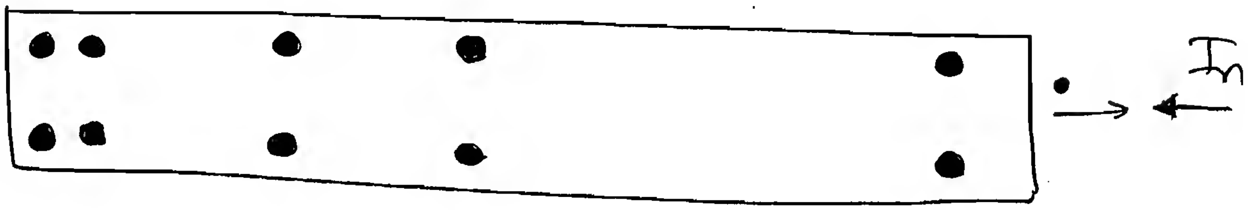


FIG - 2

$\Rightarrow$ Consider an n-type Semiconductor (fig-2) with a non-zero value of Concentration gradient $\left(\frac{dn}{dx} \neq 0\right)$. Due to difference in concentration electrons ~~holes~~ diffuse from higher to lower (Left to right) Concentrated area until uniform Concentration $\left(\frac{dn}{dx} = 0\right)$ is achieved. and produced electron diffused current. where electron diffusion current density. $J_n(x)$ is given by.

$$\boxed{J_n(x) = \frac{I_n}{A} = +qD_n \frac{dn}{dx}.}$$

⇒ If a Charge Carrier moves due to difference in concentration it is said to be diffussing where as if a Charge Carrier moves due to attraction (or) repulsion of a Voltage it is said to be drifting. Diffussion current is proportional concentration gradient of Charge Carriers where as drift current is proportional to concentration of charge Carriers and electric field where drift current density J is given by

$$\Rightarrow \boxed{J = \frac{I}{A} = \sigma E = (nq\mu_n + pq\mu_p) E.}$$

⇒ D_p, D_n : Diffussion Constants for hole, electron given by

$$\boxed{\frac{D_p}{\mu_p} = \frac{D_n}{\mu_n} = V_T = KT = \frac{\bar{K}T}{q} = \frac{T^\circ K}{11{,}600} = 0.026V \quad (\text{AT } 300^\circ K)}$$

$K = eV/K$
$\bar{K} = J/K$

Einsten's Relationship

→ V_T : thermal Voltage
K : Boltzman's Constant in $eV/^\circ K$.

$\bar{K}$ = Boltzmann constant in J/°K.

T : temp. in °K.

* Hall Effect:

⇒ If a semiconductor carrying a current I_x is placed in transverse magnetic field B_z then an electric field E_y gets induced in a direction perpendicular to I_x & B_z.

⇒

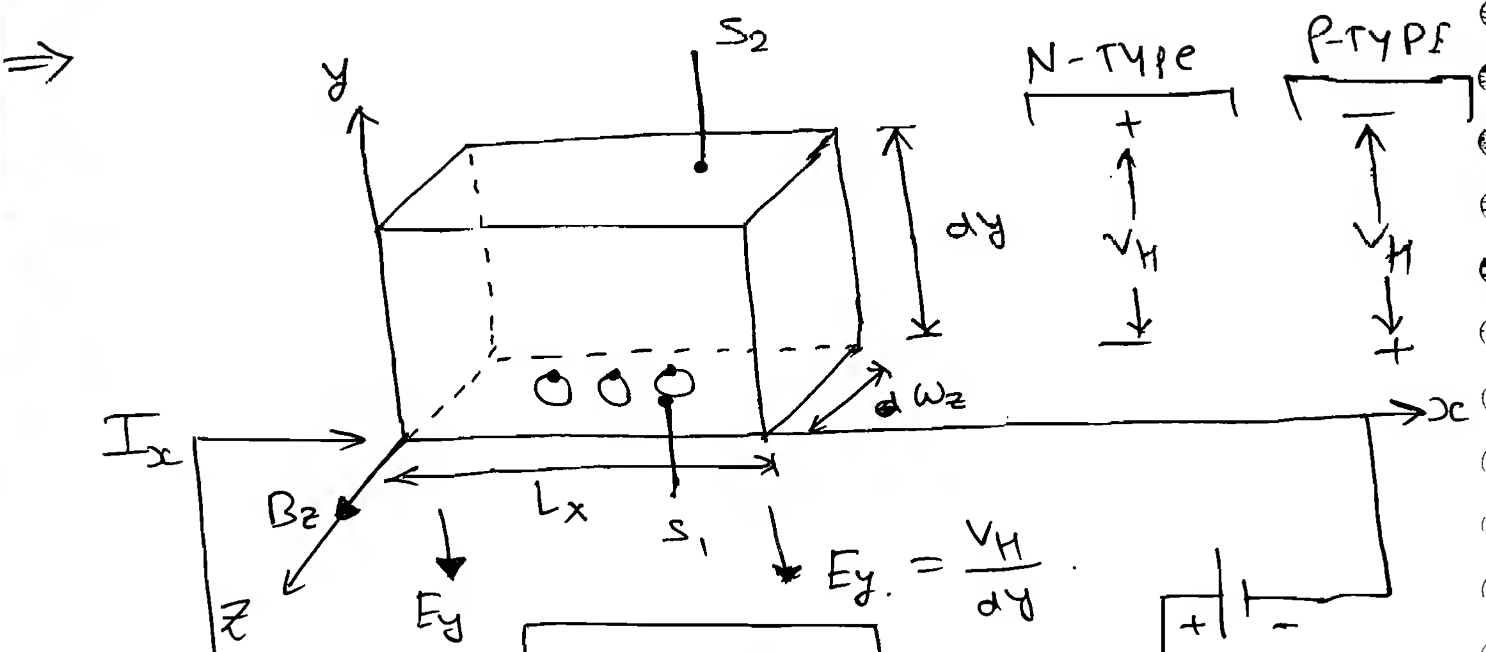


Fig. ①

$E_x = \frac{V_x}{L_x}$

S_1, S_2 : Surface-1, Surface-2.

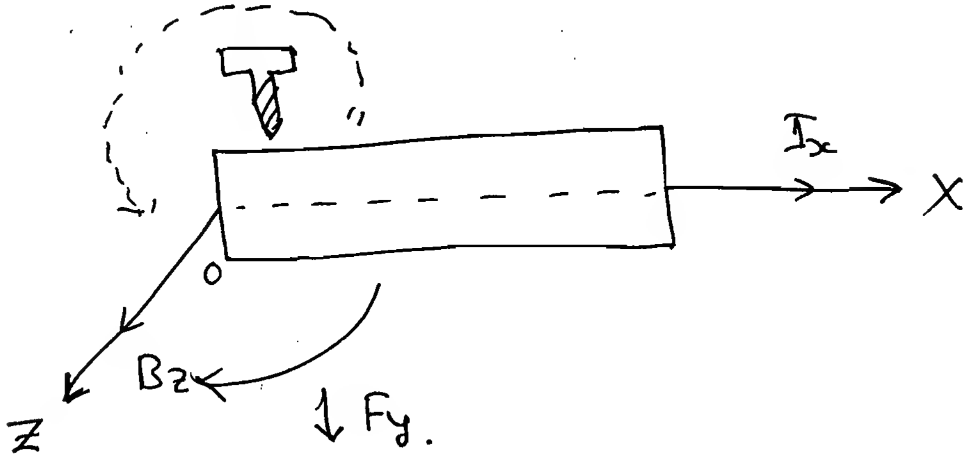
→ If a semiconductor carrying a current I_x is placed in a transverse magnetic field B_z then according a motor

Law: a force gets induced in a direction perpendicular to I_x & B_z in the direction of forward motion of a right handed screw wound from I_x to B_z.

$$\boxed{V_H = \frac{B_z \cdot I_x}{e\,\omega_z} (V).}$$

e = Charge density

⇒



⇒ Due to the induced force all the charge carriers are pulled towards a surface hence that surface becomes negetively (or) positively charged w.r.t. other surface. Hence, the potential rise (or) voltage called Hall voltage V_H gets induced along y-dimension of sample. Hence an electric field E_y gets induced along y- direction. It was proved in 1879 by Edwin Hall.

* Applications:

⇒ ① It can be used to find the type of semiconductor. (N or P type). by looking at V_H polarities.

⇒ ② It can be used to find charge density and hence carrier concentration (electron (or) Hole concentration).

$$V_H = \frac{B_z \cdot I_x}{e \cdot W_z} \rightarrow \rho =$$

N - Type : $e_n = nq \rightarrow n =$

P - Type : $e_p = pq \rightarrow p =$

⇒ ③ Given mobility, conductivity can be calculate (or) viceversa.

⇒ Hall constant (or) Hall coefficient

$$\boxed{R_H = \frac{1}{e} = \frac{V_H \cdot W_z}{B_z \cdot I_x} \ m^3/C} \longrightarrow R_H =$$

→ $\sigma = \rho\mu \longrightarrow \mu = \frac{\sigma}{e}$

σ : conductivity

e : charge density

μ : mobility.

$$\Rightarrow \boxed{\mu = \sigma R_H}$$

(4)

⇒ It can be used to multiply two signals. (Hall effect multiplier).

$\boxed{Q}$ Calculate μ_p for a p-type Germenium bar connected as in figure - 1 and is exibitting Hall effect given

$B_z = 0.1$ Wb/m²

$d_y = W_z = 3$ mm.

$V_H = 50$ mV.

$I_x = 10\ \mu A$.

$\rho = 200,000\ \Omega$-cm.

Solⁿ:

$$R_H = \frac{V_H \cdot W_z}{B_z \cdot I_x}.$$

$$\therefore R_H = \frac{50 \times 10^{-3} \times 3 \times 10^{-3}}{0.1 \times 10 \times 10^{-6}}$$

$$\therefore R_H = 150\ m^3/c.$$

$$\therefore \mu = \sigma \cdot R_H.$$

$$\therefore \mu = \frac{1}{\rho} \cdot R_H.$$

ρ → Resistivity.

$$\therefore \mu = \frac{1}{2 \times 10^3} \times 150.$$

$$\therefore \boxed{\mu = 75 \times 10^{-3}\ m^2/V\text{-}s.}$$

Note: In $R_H = \frac{1}{\rho}$ eqn ρ is Charge density where as ρ given in problem statement is Resistivity.

Q Find the magnitude of Hall Voltage V_H in an N-Type are bar connected as in fig-① and is exibutting Hall effect given.

$$N_0 = 10^{17}\ cm^{-3}.$$

$$B_z = 0.1\ wb/m^2.$$

$$d_y = 3mm$$

$$E_x = 5\ v/cm.$$

$$\mu_n = 3800\ cm^2/v\text{-}sec.$$

Soln:

$$V_H = \frac{B_z \cdot I_x}{e \cdot W_z}.$$

Note: E_x, V_x, I_x, B_z are applied quantities

F_y, V_H & E_y are induced quantities.

$$J_x = \frac{I_x}{A}.$$

Note In drift and diffussion current densities eqns, ($J = I/A$) cross sectional area A is defined as perpendicular area for current.

$$\rightarrow \boxed{J_x = \frac{I_x}{\omega_z \cdot dy} = \rho v = \rho \mu_n E_x}$$

ρ = charge density.

v = drift velocity.

→ μ : mobility

E : electric field.

$$\boxed{\frac{I_x}{W_z} = \rho \mu_n E_x dy} \quad — (2).$$

Sub. eq (2) into (1).

$$V_H = \frac{B_z}{\cancel{\rho}} \cdot \cancel{\rho} \mu_n E_x dy.$$

$$\therefore \boxed{V_H = B_z \cdot \mu_n \cdot E_x \cdot dy.}$$

$$\therefore V_H = 0.1 \times 3800 \times 10^{-4} \times 5 \times 10^{2} \times 3 \times 10^{-3}.$$

$$\therefore V_H = 5700 \times 10^{-5}$$

$$\therefore \boxed{V_H = 57 \, mV.}$$

Q A p-type silicon speciman is exibitting Hall effect and is connected as in fig-(1) calculate induced Voltage given

B_z = 0.1 wb/m².

E_y = 750 V/m.

dy = 0.009 m.

Soln:

$\Rightarrow$ $V_H = E_y \cdot dy$

$= 750 \times 0.009$

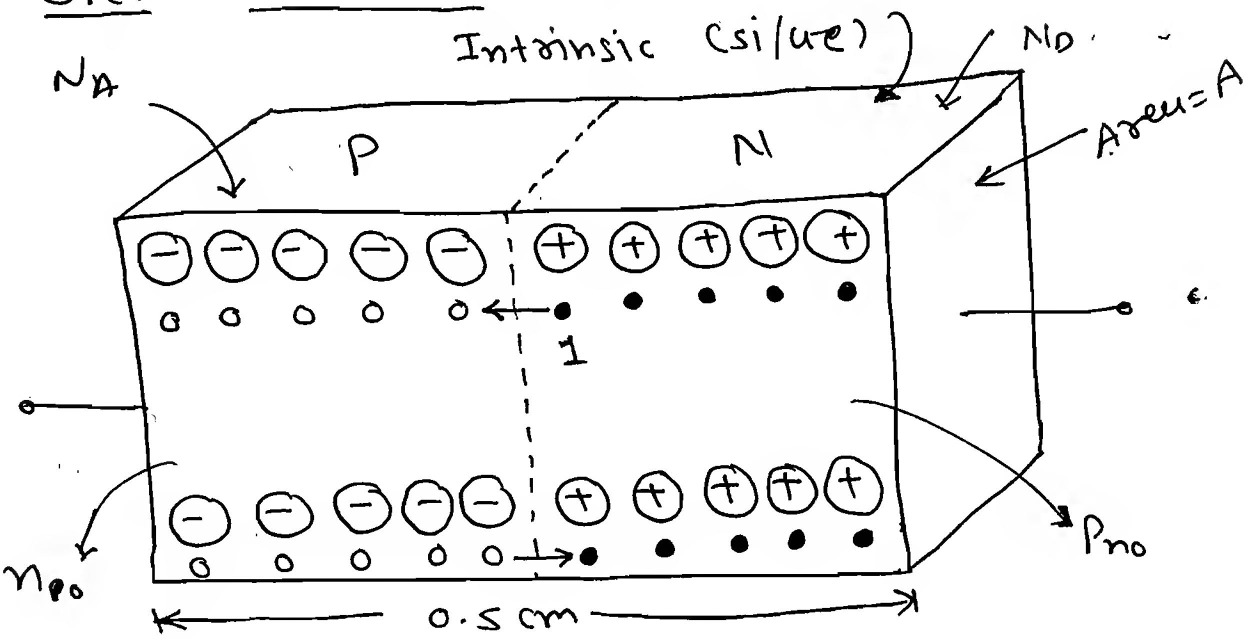
$\therefore \boxed{V_H = 6.75V}$

☆ P-N Junction Diode:

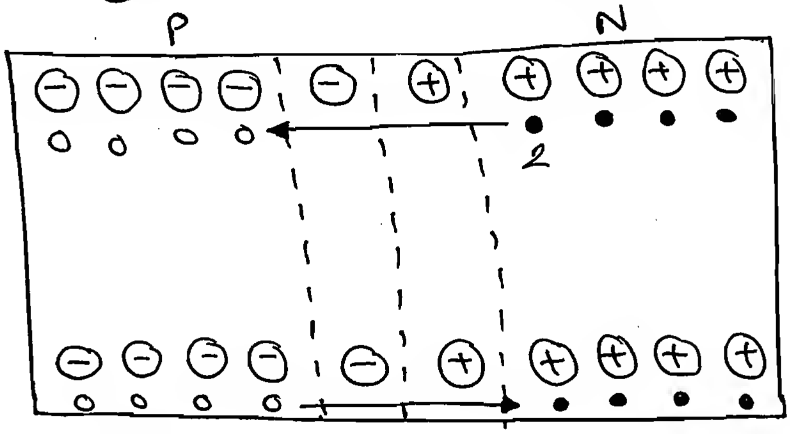
* Open circuited P-N Diode:

☆ P-N Junction Diode:

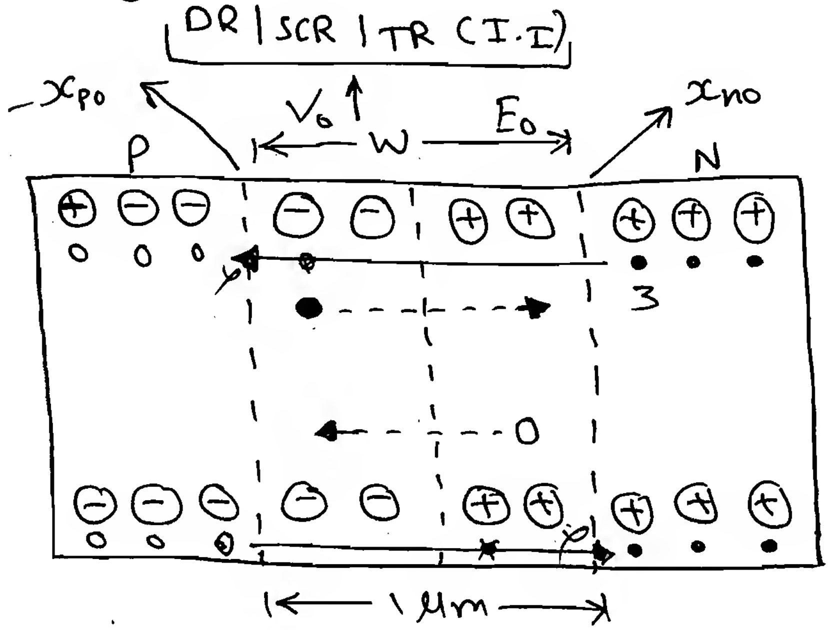
* Open circuited P-N ~~Junction~~ Diode:



Ⓐ Without Barrier.



Ⓑ



Ⓒ With Barrier.

n_{p0}, P_{n0} : Initial thermally generated minority carrier concentration.

⊕• : Donor atom with excess electron (Nutral).

⊕ : Donor Ion (+ve charge).

• : Excess electron.

⊖o : Acceptor atom with excess hole. (Nutral).

⊖ : Acceptor Ion (-ve charge).

o : Excess Hole.

⇒ Fig- (A) shows internal structure of an open circuited P-N Diode which is just then created.

* <u>First explanation for formation of barrier.</u>

⇒ In fig-(A) due to difference in concentration diffussion of charge carriers start. Hence EHP recombination occurs hence +ve & -ve ions get created at centre hence fig-(A) becomes (B). In fig-(B) past diffussion oppositses present diffussion Indirectly. Though oppossion exist since concentration gradient of charge carrier is large

with difficulty diffussion may continue. Hence again recombination occurs and again Ions get created. Hence fig-(B) becomes (C). As diffussion continuous opposition to further diffussion increases. Hence after some time diffussion comes to halt. (fig-(C)).

→ The central +ve & -ve immobile ions (I.I) oppose diffussion hence called barrier. The size of barrier (1 μm) is very small compare to size of diode (~~xxxx~~ 0.5 cm). Barrier is not having charge carriers. & hence called depletion region (D.R). Barrier is the only region having Ions hence called space charge region (SCR). Barrier is separating two Nutral areas hence called Transition region (T.R).

→ W : widen of depletion region

x_{no}, x_{po} : Penetration of depletion region into n, p sides.

→ From fig-(C)

$$\boxed{W = x_{no} - (-x_{po}) = x_{no} + x_{po}} \quad —(1)$$

⇒ $\boxed{\text{Two}}$ Electr$\boxed{\text{ode}}$s

DIODE

* Application:

1. Switch.
2. Voltage Variable capacitor.

→ Barrier opposes the flow of majority carriers but supports the flow of minority carriers

*

Direction of Flow of charge carrier.	Type of current	Direction of current.
⇒ ←	e^- diffusion	→ X
⇒ →	Hole diffusion	→ X
⇒ - - - - →	e^- DRIFT	← - - - - Y
⇒ ← - - - -	Hole DRIFT	← - - - - Y

⇒ Majority carrier gives diffusion current (solid line).

⇒ Minority carriers give drift current (dotted line).

→ X : Net diffussion current (e^- + hole diffussion).

→ Y : Net Drift current (e^- + hole drift).

→ Z : Net current = X − Y.

* <u>Second explanation for formation of Barrier:</u>

⇒ Drift current opposes diffussion current But if drift less than diffussion, diffussion continuous. If diffussion continuous then EHP recombination occurs and ions get created at centre which attract minority carrier and increases drift current. As long as drift is less than diffussion, diffussion continuous. As long as diffussion continuous, drift goes on increases. At some time drift and diffussion become equal in magnitude but since opposite in direction net current becomes zero. i.e. diffussion comes to a halt. (fig ⓪).

→ Accross +ve and -ve ions existing inside depletion region internally electric flux lines get developed which induced a voltage V_0 (or) electric field E_0 which are responsible for drift current.

→ Open circuited contact Potential,

$$\boxed{V_0 = KT \ln (N_D N_A / n_i^2)} \ (V) \quad \text{---} \ (2).$$

→ Open circuited electric field intensity,

$$\boxed{E_0 = -\frac{q N_D x_{no}}{\epsilon} = -\frac{q N_A \cdot x_{po}}{\epsilon}.} \ (V/m) \quad (3).$$

⇒ Total -ve charges lost in the depletion region of n-side is equal to total +ve charges lost in the depletion region of p-side.

$$N_D x_{no} \cancel{A}\cancel{q} = N_A x_{po} \cancel{A}\cancel{q}.$$

$$\Rightarrow \boxed{N_D x_{no} = N_A \cdot x_{po}} \quad \text{---} \ (4).$$

$$\Rightarrow \boxed{x_{no} = \frac{W N_A}{N_D + N_A}} \ \text{---} \ (5) \qquad \boxed{x_{po} = \frac{W N_D}{N_D + N_A}} \ \text{---} \ (6)$$

$$\Rightarrow \boxed{\omega = \sqrt{\frac{2 \epsilon V_B}{q}\left[\frac{1}{N_D} + \frac{1}{N_A}\right]}} \quad — ⑦.$$

⇒ Penetration of depletion region into n-side is proportional to dopping of p-side. and vice-versa.

$V_B = V_0 - V$ ← +ve → F.B. ; −ve → R.B

V_0 : Built in Potential (or) Barrier (or) contact Pot.

V : applied Voltage

Note - ①:

⇒ Depletion region penetrates equally into n- & p-sides for equal doppings. & it penetrates unequally for unequal doppings.

$$N_D = N_A \longrightarrow x_{no} = x_{po}.$$

$$N_D \neq N_A \longrightarrow x_{no} \neq x_{po}.$$

Note -②:

⇒ Depletion region penetrates more into lightly dopped side.

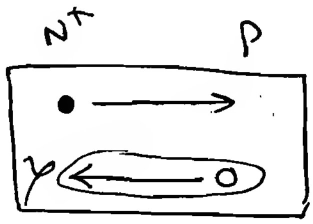
$$N_D > N_A \longrightarrow x_{po} > x_{no}.$$

Note - ③

⇒ penetration of depletion region into heavily dopped side of a single sided (or) one sided diode can

be neglected.

→ In one sided diode, one side is heavily dopped compared to other side hence most of the current is given by only one side. i.e. heavily dopped side.

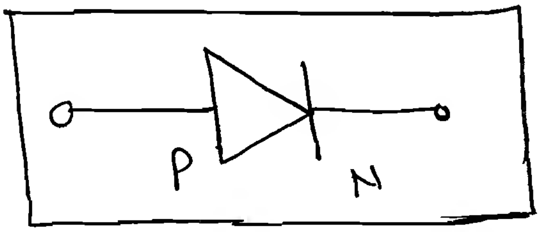
→ 

$$x_{po} = \frac{W N_D}{N_D + \cancel{N_A}} \simeq W$$

$N_D >> N_A$

$$W = x_{no} + x_{po}$$

$$\rightarrow \boxed{x_{no} \simeq 0}$$

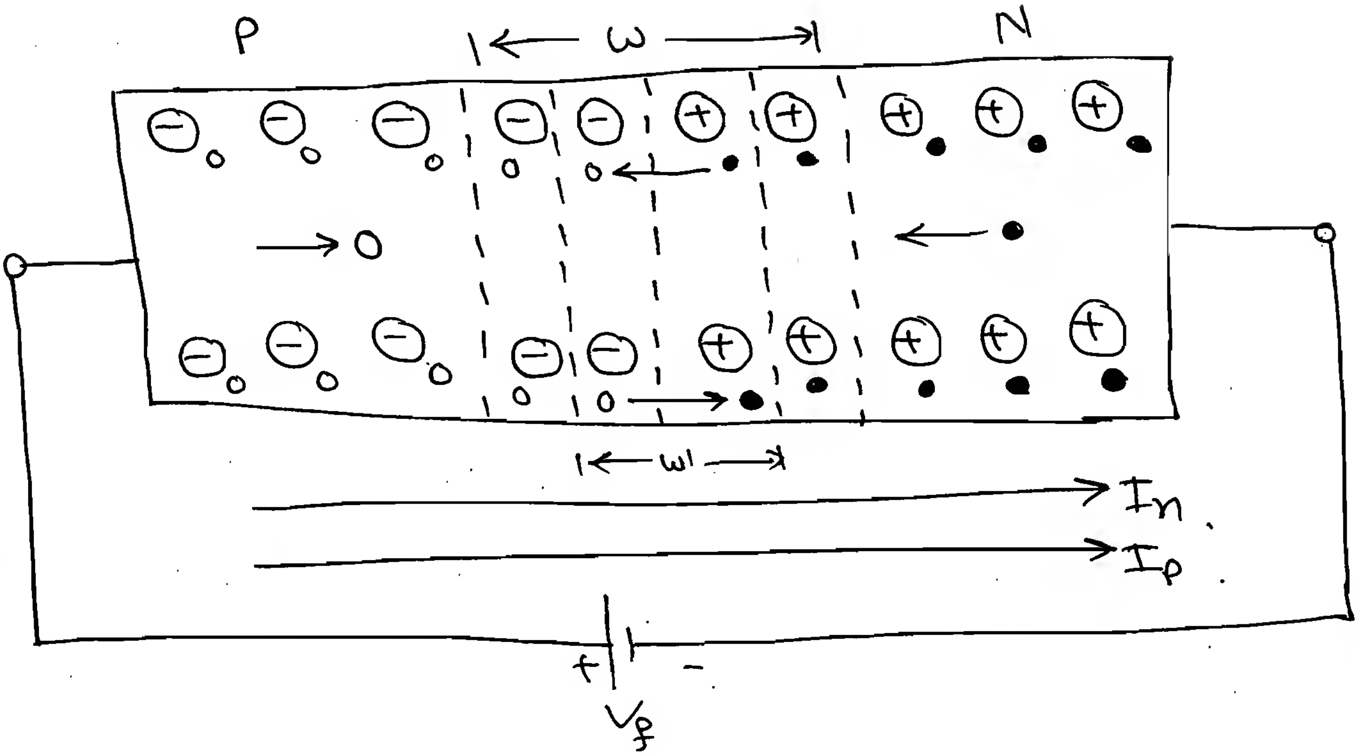
→ 

→ A circuit symbol should identify the no. of terminals and names of terminal.

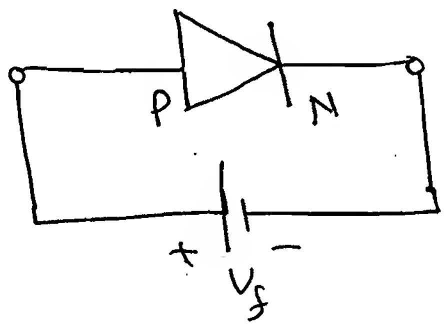
→ Vertical line represents N, triangular peace represent P. The direction of arrow shows the direction of current when the Diode is forward biased.

* Forward Biased:

=>



=>



=> If the Voltage given to p-side is more positive than n-side then diode is said to be Forward biased.

=> Due to Polarities of forward biased Charge carriers get repelled and enter into open circuited depletion region due to which immobile ions get back their lost charge carriers become nutral and move to undepleted

region hence width of depletion region decreases (W') compared to open circuit (W). Due to decrease in ions V_o (V) and E_o (eV) decrease by V_f.

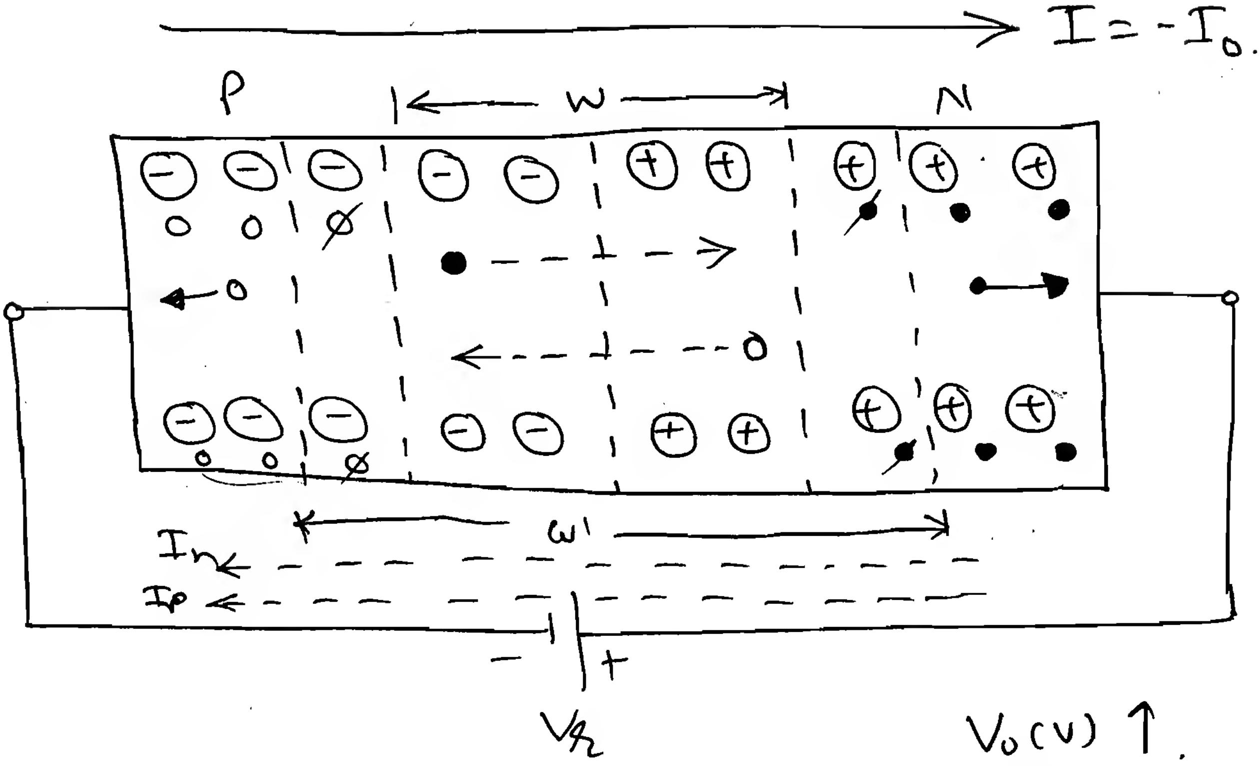
⇒ Cut-in Voltage (or) offset voltage (or) break-point voltage (or) threshold voltage (or) firing point voltage V_γ is defined as minimum forward bias to be given across a p-N junction for current to exist.

⇒ Majority carrier diffusion supports flow of currents. Hence magnitude of current is large is (mA (or) A) and the direction is from p to N.

⇒ To the left and right drift current exist. To the centre diffusion current exist. But diffussion is important. Using which central barrier can be crossed which was oppossing current in open circuit case.

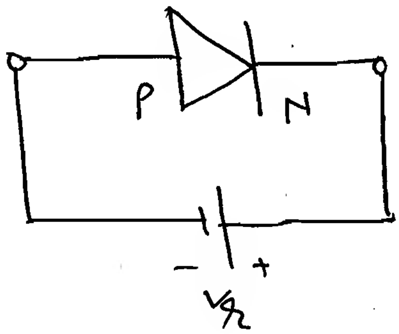
* Reverse Biased:

⇒ $I = -I_0$.



V_0 (V) ↑.
E_0 (V) ↑.

⇒



⇒ Due to Polarities of reverse biased nutral atoms adjusted to open circuited depl region loose charge carriers become immobile ions and move to depletion region hence width of depletion region increases (W') compared to open circuit (W).

⇒ Due to increase in Ions V_0 (Volts) and E_0 (eV) increase by V_R.

→ Minority carrier drift support flow of current hence less current, μA for Ge and nA for Si flows. Direction is N to P.

→ Increase in reverse bias, increases width of depletion region but thermally generated minority carriers are constant. Hence, reverse current is independent of reverse voltage called Reverse Saturation current I_o. i.e.

$$\frac{dI_o}{dV} = 0.$$

→ I_o physically flows from N-to-P but shown P-N. hence negative.

⇒ Increase in temp. increases EHP generation and minority concentration hence I_o increases. i.e.

$$\frac{dI_o}{dT} > 0$$

* Volt - Ampere (V - I) characteristics:

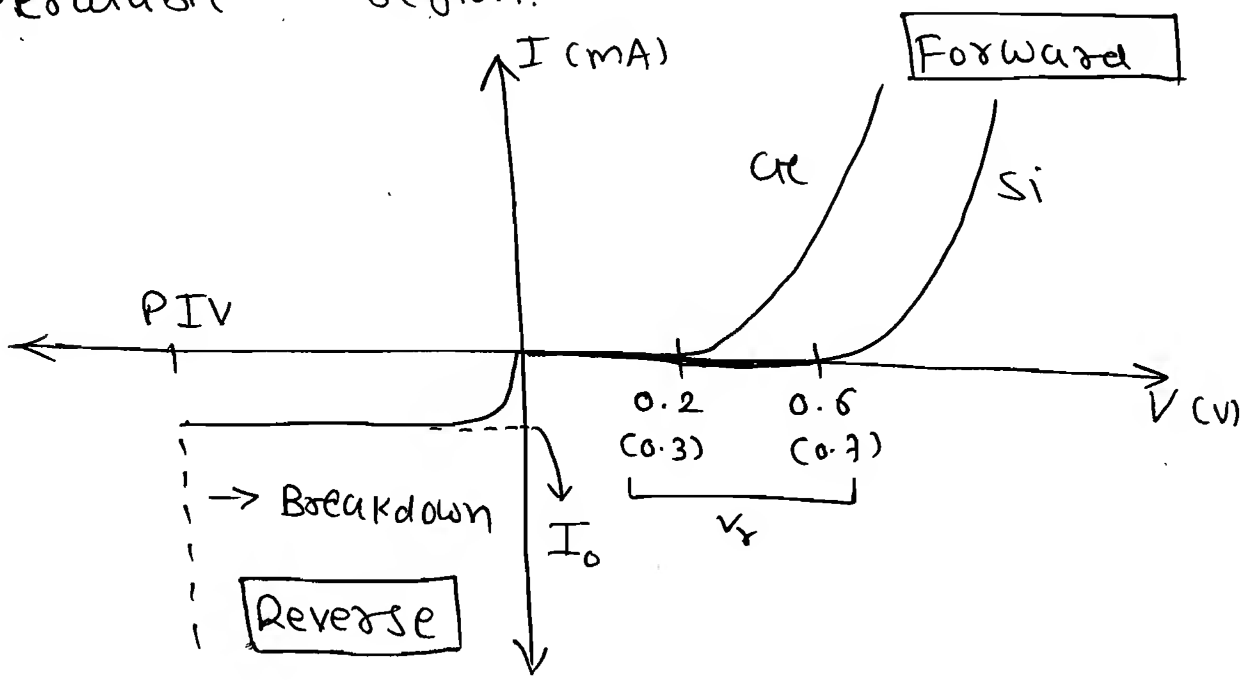
⇒ I is defined as current flowing through the diode from P- to N.

⇒ V is defined as Voltage across terminals of Diode with positive at P side.

⇒ Peak - Inverse Voltage (P_{IV}) is defined as maximum reverse bias that can be safely applied across a P-N diode.

⇒ Dotted line in the graph is non-operatable region.

⇒



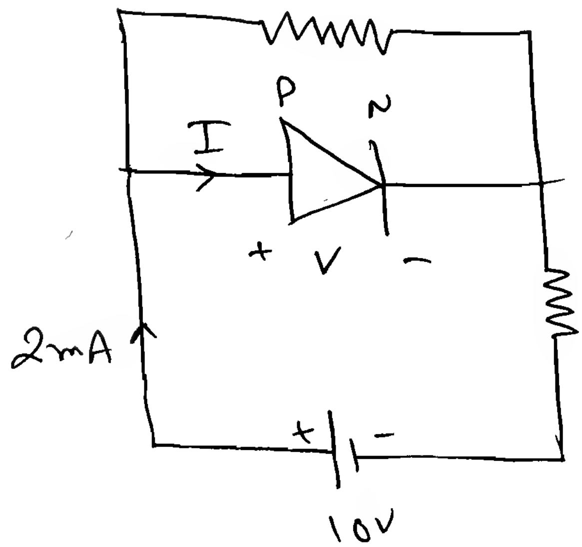
⇒ $$\boxed{I = I_o \left(e^{V/\eta V_T} - 1\right)}$$

$\eta = 1$ Ge.

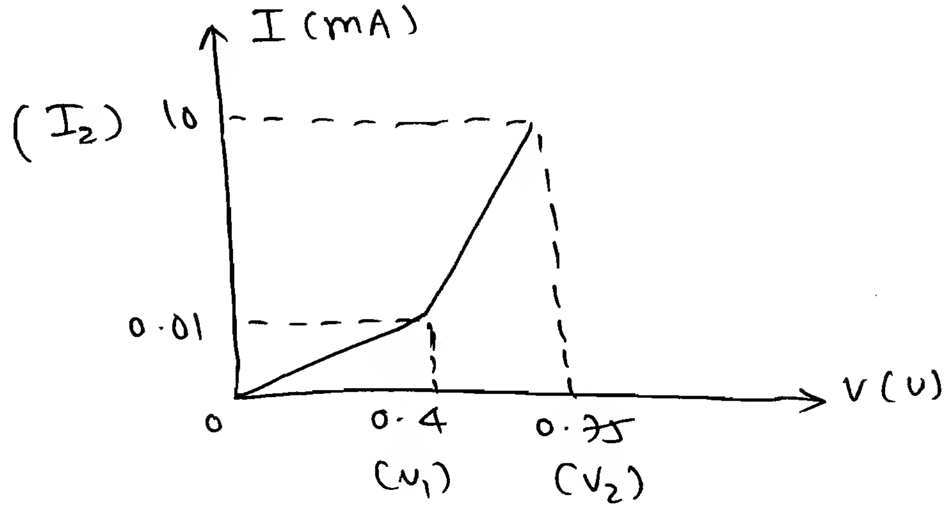
$= 2$ Si.

$\boxed{FB}$: $V = +ve$: If $e^{V/nV_T} >> 1$ Then $I = I_o e^{V/nV_T}$

$\boxed{RB}$: $V = -ve$: if $e^{V/nV_T} << 1$ then $I = -I_o$.



$\boxed{Q}$ Given V-I Characteristics of P-N Diode Comment on weither it is Si or Ge Diode?



Soln: Current eqn of diode is modified to a ratio

$$\frac{I_2}{I_1} = \frac{I_o(e^{V_2/nV_T} - 1)}{I_o(e^{V_1/nV_T} - 1)}.$$

$$\therefore \frac{10}{0.01} = \frac{e^{V_2/n\gamma_T}}{e^{V_1/n\gamma_T}}$$ ($\because$ neglect -1)

$$\therefore 1000 = e^{\frac{(V_2-V_1)}{nT}}$$

$$\therefore 1000 = e^{\frac{0.35}{n \times V_T}}$$

$$\therefore 6.9 = 0.35 \times \frac{1}{n \times 0.026}$$

$$n = \frac{13.46}{6.9}$$

$\therefore \boxed{n = 1.95} \simeq 2.$ is mathes for silicon.

So, Diode is made up of silicon.

Note:

$\rightarrow$ For Practical application ~~is~~ prefered

Si diode is prefered than Ge diode

due to following reason.

① I_o of Ge (μA) > I_o of Si (nA)

$\rightarrow$ Hence si diode act as better switch.

② E_G of Ge < Si.

$\rightarrow$ Hence, Si diode gives better opeatuble thermal range.

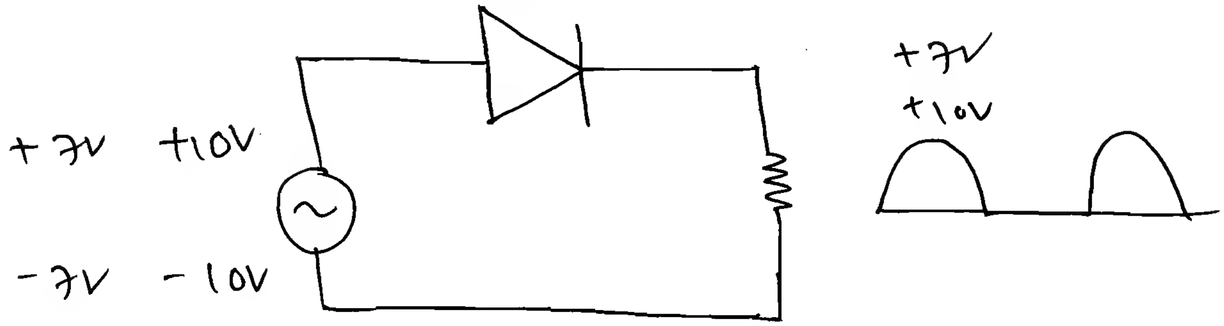
	Switch Ge	Si
300 K :	✓	✓
400 K :	X	✓
500 K :	X	X

③ PIV of Ge < Silicon.

→ Hence, si diode gives better operatable range.

Ge (PIV = 7V)

Si (PIV = 10V)



④ For si Diode abundant raw material available.

→ Reasons ①, ② & ③ are called primary reason and ④ is secondary reason.

→ The above explanation is valid for any electronic device as specially high power devices like SCR, DIAC, TRIAC etc. will be made up of si since si can withstand higher temp.

* Diode Resistances:

→ DC (or) Static Resistance,

$$\boxed{R_{DC} = \frac{V}{I}}$$

→ Ac (or) Dynamic Resistance,

$$\rightarrow r_{ac} = \frac{dV}{dI} = \frac{1}{TAN\phi} = \frac{1}{\tan\phi}.$$

→ $r_{ac} = (\eta V_T / I)$ ⟶ For F.B. only.

$r_{ac} = \frac{\eta V_T}{I_0} \cdot e^{-V/\eta V_T}$ ⟶ (For F.B & V = +ve
R.B. V = −ve)

Q A Ge diode has $I_0 = 30\mu A$ at 125°C. Find dynamic resistance under pass

(i) Forward biased of 0.2 V.

(ii) Reverse biased of 0.2 V.

Soln:

$$r_{ac} = \frac{\eta V_T}{I_0} \cdot e^{-V/\eta V_T}$$

$\eta = 1$, ~~V_T = 0.026V~~, $I_0 = 30\mu A$

Note: $V_T = 0.026\text{ V}$ is valid only at 27°c. At 125°C $\boxed{V_T = \frac{T^\circ K}{11,600}}$

$$\therefore \quad V_T = \frac{273^{\circ}K + 125}{11,600}$$

$$V_T = 0.0343\ V$$

(i) $V = +0.2V$

$$r_{acf} = \frac{\eta V_T}{I_0} \cdot e^{\frac{V}{-\eta V_T}}$$

$$= \frac{1 \times 0.0343}{30 \times 10^{-6}} \cdot e^{-\frac{0.2}{1 \times 0.0343}}$$

$$\boxed{r_{acf} = 3.356\ \Omega}$$

(ii) $V = -0.2\ V.$

Remember

$$\therefore \quad r_{acR} = \frac{1 \times 0.0343}{30 \times 10^{-6}} \cdot e^{\frac{0.2}{1 \times 0.0343}}$$

$$\boxed{r_{acR} = 3.89 \times 10^{5}\ \Omega}$$

$$\therefore \quad \boxed{r_{acR} = 389.5\ K\Omega}$$

(a) The reverse biused Saturation Current of a silicon P-N diode is $1\mu A$. determine its a.c. resistance if 0.4 V of forward biuse is applied.

Solⁿ:

$$r_{ac} = \frac{\eta V_T}{I}$$

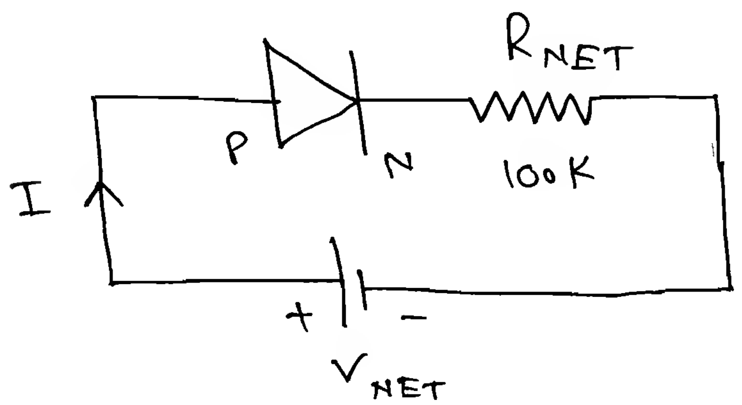
$$\Rightarrow \quad r_{ac} = \frac{n V_T}{I_o\left(e^{V/nV_T} - 1\right)}$$

$$= \frac{2 \times 0.026}{10^{-6} \times \left(e^{\frac{0.4}{2\times 0.026}} - 1\right)}$$

$$\therefore \boxed{r_{ac} = 23.74\ \Omega}$$

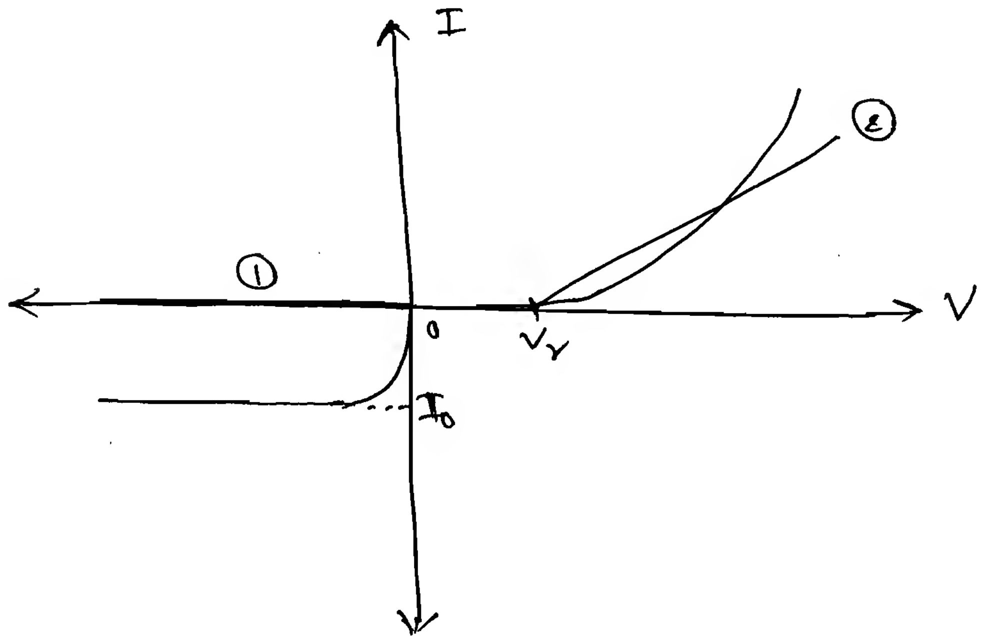
* Equivalent circuit:

$\Rightarrow$



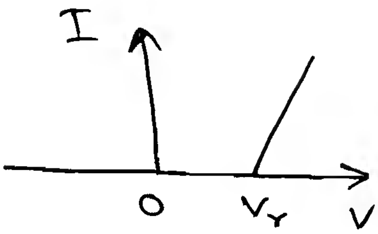
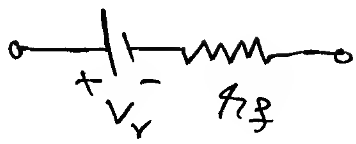
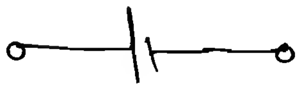
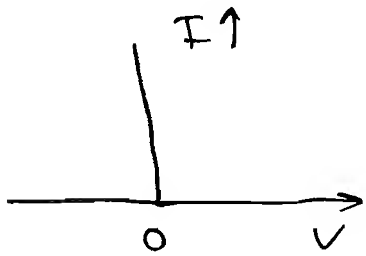
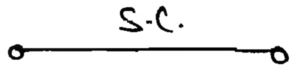
$\Rightarrow$ R_{NET}, V_{NET} : Resistance, Voltage of a N/W.

$\Rightarrow$



V vs I

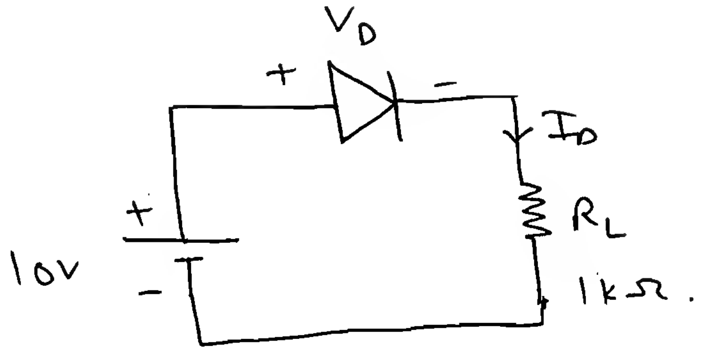
*

Name	Characteristics	Equivalent Ckt	Condn
① Piecewise Linear model			~~$R_{NET} \gg r_f$~~
② Simplified piecewise linear model			$R_{NET.} \gg r_f$
③ Ideal Model			$R_{NET.} \gg r_f$ $V_{NET.} \gg V_\gamma$

⇒ In the above equivalent ckt +ve of V_γ should match with P-side of diode.

⇒ The above eqn ckt are valid only for forward biased diode for a reverse bias diode eqn ckt in all the three model is open ckt.

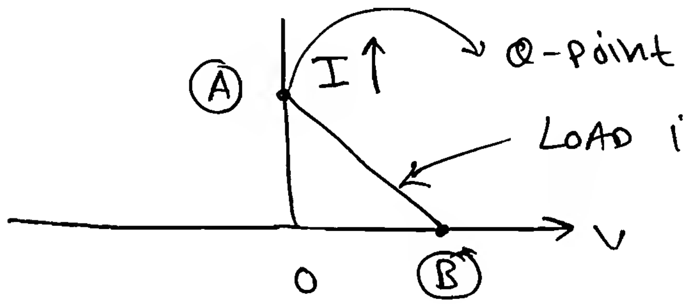
$\boxed{Q}$ Determine Q-point in the given ckt. Assume ideal diode.



Solⁿ:

Note:

→ Q-point is defined as intersection of load line with V-I chara.



By KVL,

$$\therefore \quad 10 = V_D + 1000\, I_D.$$

→ $V_D = 0$

So, $10 = 0 + 1000\, I_D$

$\boxed{I_D = 10\,mA}$ (: A).

→ $I_D = 0$.

So, $\boxed{V_D = 10\,V}$ (: B).

⇒ Slope of AB line is controlled by load R/k R_L. hence called load line.

Q-point $= (V_{DQ}, I_{DQ}) = (0, 10\,mA)$.

Q) A diode whose V-I characteristics as shown in fig-a is connected as in fig-b calculate I'.

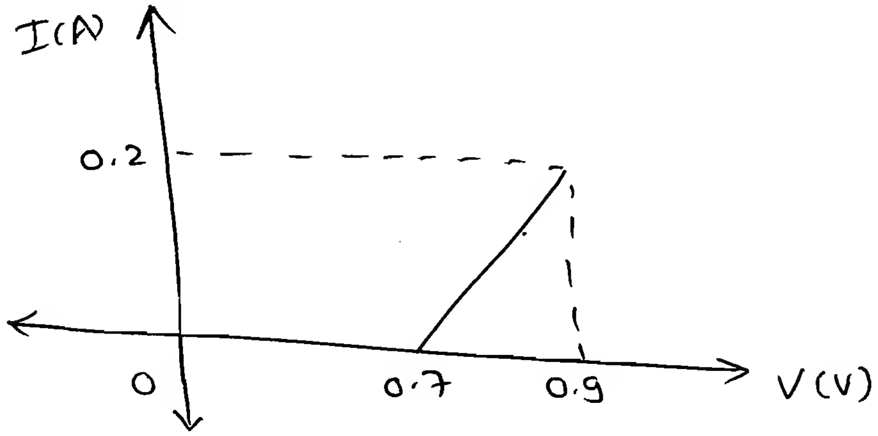
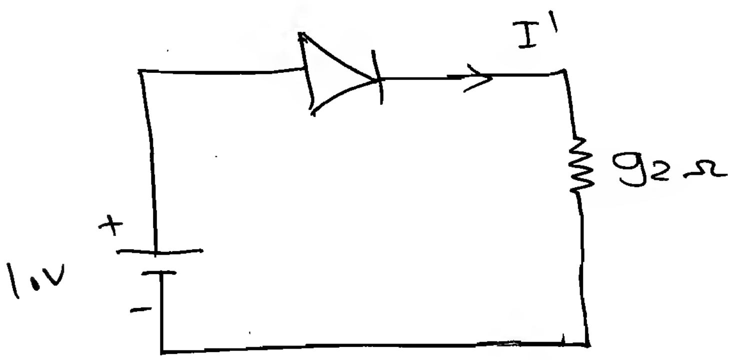


fig-(a)

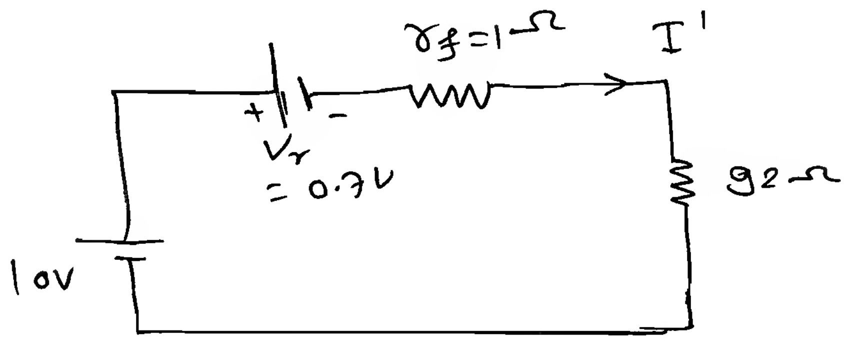


Sol^n:

$V_\gamma = 0.7\ V$

$r_f = \frac{(0.9 - 0.7)\ V}{(0.2 - 0)\ A} = \frac{0.2}{0.2} = 1\ \Omega.$

eq^n ckt:



By KVL,

$10 - 0.7 = I'(1 + 92).$

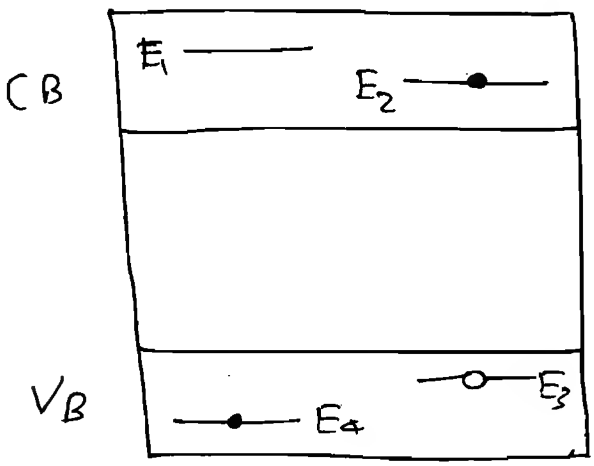
$\therefore I' = 9.3/93 = 0.1\ A$

$\boxed{I' = 0.1A}$

* Fermi level:

⇒ Existing electron in conduction band and non-existing electron in valance band both can support current. Hence to comment on conductivity of a semiconductor we should be able to know the existance (or) non-existance of electron at a given energy level. To comment on this, Fermi dirac distribution (or) Fermi dirac probability distribution is define as.

$$\boxed{f(E) = \frac{1}{1 + e^{(E-E_F)/KT}}} \quad \text{——— (1)}$$



$f(E_1) = 0$

$f(E_2) = 1$

$f(E_3) = 0$

$f(E_4) = 1$

⇒ $f(E)$ Probability of existance of electron at an allowed energy level E

$(0 \leq f(E) \leq 1)$.

→ E_F : Fermi energy level (imaginary).

Comments on 50% occupancy.

→ K : Boltzman constant in eV/°K.

T : Temp. in °K.

* Fermi level in Intrinsic semiconductor

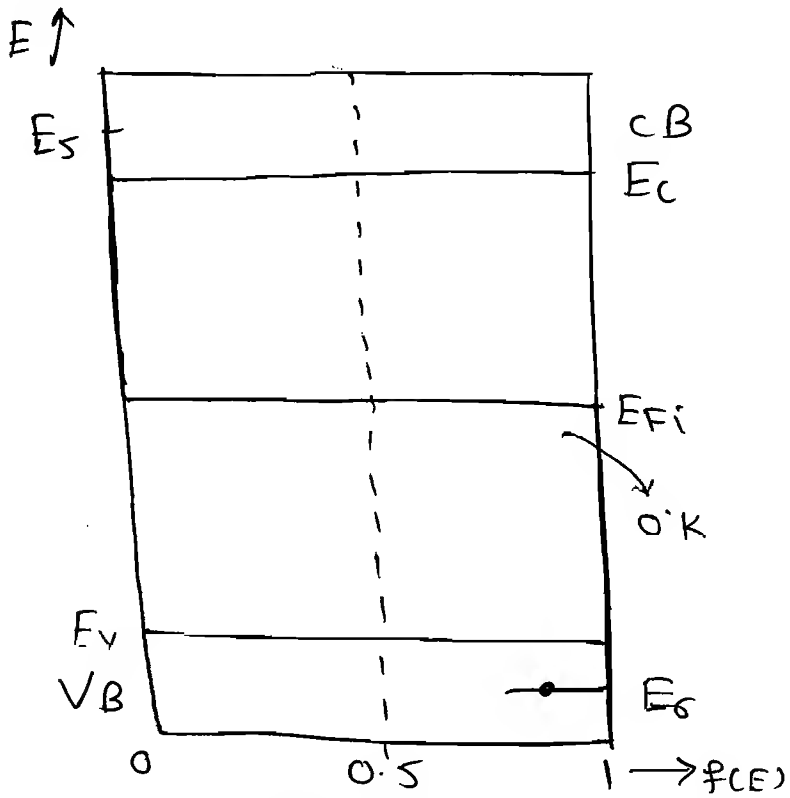


FIG ①

⇒ T = 0°k

$$E > E_F \longrightarrow f(E) = \frac{1}{1+e^{+\infty}} = 0.$$

$$E < E_F \longrightarrow f(E) = \frac{1}{1+e^{-\infty}} = 1.$$

⇒ T ≠ 0°k

$$E = E_F \longrightarrow f(E) = \frac{1}{1+e^{0}} = \frac{1}{2} \text{ (OR) } 50\%$$

→ At 300 K EHP generation occurs and electron goes to conduction band leaving a hole in valance band as in fig-②

⇒

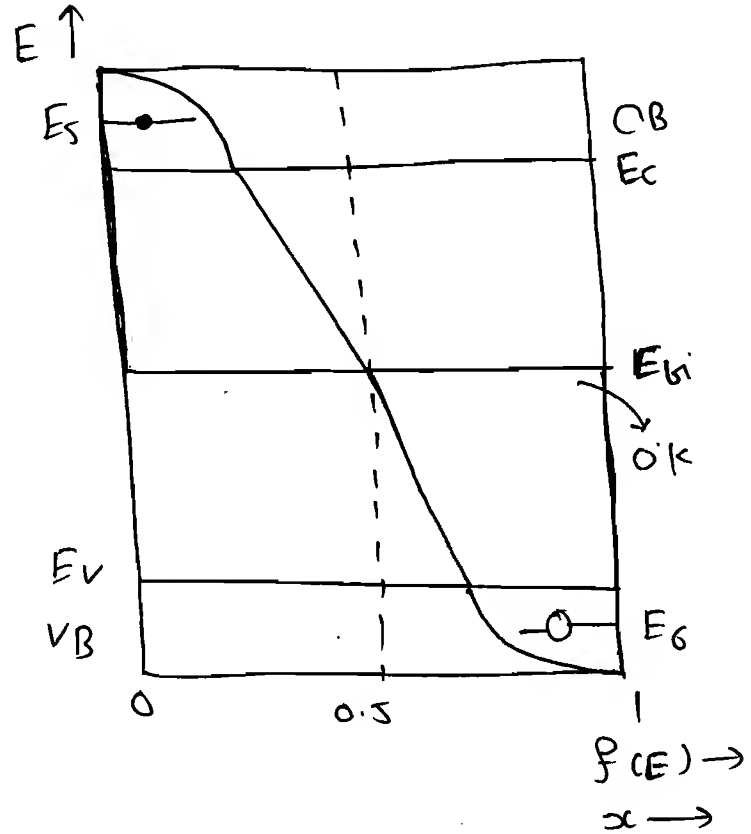


Fig-②

→ By integrating f (E) fn along with other the term with $E > E_c$ we get free electron concentration n

$$\boxed{n = N_c\, e^{-(E_c - E_F)/kT}} \quad \text{——— ②}$$

where

$$\boxed{\begin{aligned} N_c &= 2\,(2\pi m_n \bar{k} T / h^2)^{3/2} \\ &= 4.8 \times 10^{15}\, (m_n T / m)^{3/2} \ \mathrm{cm}^{-3} \end{aligned}} \quad \text{— ③}$$

→ $1-f(E)$ is Prob. of non existance of electron at an energy level E in conduction band (or) valance band. It is also prob. of existance of hole at an energy level E in valance band only.

⇒ By integrating $1-f(E)$ fn along with some other terms with $E \leq E_V$ we get hole concentration P,

$$\rightarrow \boxed{P = N_V \cdot e^{-(E_F - E_V)/kT}} \quad \text{———} \quad (4)$$

$$\rightarrow \boxed{\begin{aligned} N_V &= 2\,(2\pi m_p \bar{k} T / h^2)^{3/2} \\ &= 4.82 \times 10^{15}\,(m_p T/m)^{3/2}\ \text{cm}^{-3} \end{aligned}} \quad \text{—} (5).$$

→ N_c, N_v : Densities of energy states at conduction, valance Band. They are constants dependent on temp. and independent of dopping.

→ m_n, m_p : effective mass of electron, hole.

→ m : mass of electron.

→ k : Boltzman constant in eV/°K.

→ $\bar{k}$: Boltzman constant in J/°K.

→ T : Temp. in °K.

→ h : plank's constant.

⇒ For intrinsic semiconductor $n=p$. Substitute in ② & ④ we get,

$$\boxed{E_{Fi} = \left(\frac{E_c + E_v}{2}\right) - \frac{KT}{2} \ln\left(\frac{N_c}{N_v}\right)} \quad \text{——} \quad ⑥$$

⇒ If $m_n = m_p$, then

$$\boxed{E_{Fi} = \frac{(E_c + E_v)}{2}} \quad \text{——} \quad ⑦$$

i.e. intrinsic fermi level lies at the centre of forbidden band if $m_n = m_p$.

→ It lies above (or) below the centre if $m_n \neq m_p$.

→ Substituting ② & ④ in ⑦, to $n \cdot p = n_i^2$ we get.

$$\rightarrow \boxed{E_G = KT \ln\left(\frac{N_C \cdot N_V}{n_i^2}\right)} \quad \text{--- (8)}$$

* Fermi level in Extrinsic semiconductor

→ At room temp. probability of existance of electron in conduction band of n-type semiconductor is more than prob. of existance of electron in conduction band of intrinsic semi-conductor. Hence, fermi level moves closer to conduction band in n-type then intrinsic.

⇒ For n-type semiconductor $n_n \simeq N_D$.

from eqn - (2)

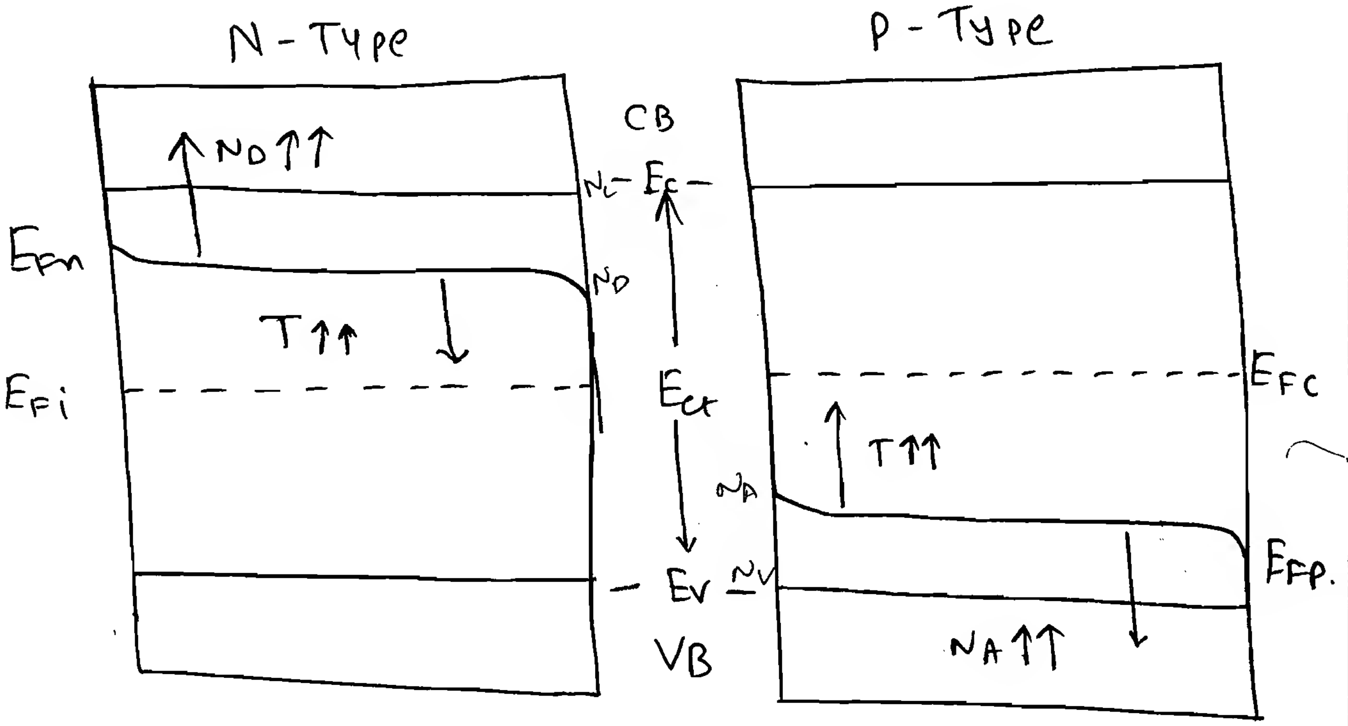
$$\boxed{E_{Fn} = E_c - KT \ln(N_c/N_D)} \quad \text{--- (9)}$$

⇒ For p-type semiconductor $P_p \simeq N_A$.

from eqn - (4)

$$\boxed{E_{Fp} = E_V + KT \ln(N_V/N_A)} \quad \text{--- (10)}$$

→ As dopping concentration increases in n-type ~~[illegible]~~ (p-type). Fermi level moves closer and closer to conduction band (valance band) and may coinside with edge of conduction band E_c (edge of valance band E_v) and may even penetrate into conduction band (valance band).



⇒ <u>N- Type:</u>

(300°K)

$$E_{Fn} = E_c - kT\ln\left(\frac{N_c}{N_D}\right).$$

N_D : $N_D < N_c \longrightarrow E_{Fn} < E_c$.

$N_D\uparrow$: $N_D = N_c \longrightarrow E_{Fn} = E_c$.

$N_D\uparrow\uparrow$: $N_D > N_c \longrightarrow E_{Fn} > E_c$.

→ As Temp. increases Fermi level moves closer to centre of forbidden band in both n- & p-type semiconductors.

→

$$\boxed{\begin{aligned} E_{Fn} - E_{Fi} &= kT \ln (N_D/n_i) \\ E_{Fi} - E_{Fp} &= kT \ln (N_A/n_i) \end{aligned}}$$

— (11)
— (12)

$\boxed{Q}$ In a P-type semiconductor fermi level lies 0.04 eV above valance band. find New location of fermi level if acceptor concentration is doubled.

Sol^n: equating P_p to N_A in eq^n - (4) we get.

$$N_A = N_V \cdot e^{-(E_F - E_V)/kT}$$

$$\therefore \frac{N_{A1}}{N_{A2}} = \frac{e^{-(E_{FP1} - E_V)/kT}}{e^{-(E_{FP2} - E_V)/kT}}$$

$N_{A2} = 2N_{A1}$

$$\therefore 2 = e^{-\left(\frac{E_{FP2} - E_V}{kT}\right) + \left(\frac{\overbrace{E_{FP1} - E_V}^{0.04\,eV}}{kT}\right)}$$

$$e^{-\frac{0.04\,eV}{0.026}} \times 2 = e^{-\frac{(E_{FP2} - E_V)}{kT}}$$

$$\therefore e^{-\frac{(E_{FP2} - E_V)}{kT}} = 2 \times 0.2145.$$

$$\therefore \quad 2.33 = e^{\frac{(E_{FP2} - E_V)}{KT}}$$

$$\therefore \quad \boxed{E_{FP2} - E_V = 0.022\,eV.}$$

Ans: New fermi level lies 0.022 eV above E_V.

Q In n-type semiconductor Fermi level lies 0.3 eV below E_C at 300 K. Find new location of fermi level at 330 K. Assume N_C to be constant.

Soln:

$$E_C - E_{Fn} = 0.3\,eV.$$

from eqn – 9

$$E_C - E_{Fn} = KT \ln\left(\frac{N_C}{N_D}\right).$$

$$\therefore \frac{E_C - E_{Fn2}}{E_C - E_{Fn1}} = \frac{\cancel{K}T_2 \ln\cancel{\left(\frac{N_C}{N_D}\right)}}{\cancel{K}T_1 \ln\cancel{\left(\frac{N_C}{N_D}\right)}}$$

$$\therefore \frac{E_C - E_{Fn2}}{0.3\,eV} = \frac{330}{300}$$

$$\therefore \quad \boxed{E_C - E_{Fn2} = 0.33\,eV.}$$

Ans: New fermi level lies 0.33 eV below E_C.

☆ Fermi Level in open circuited P-N Diode :

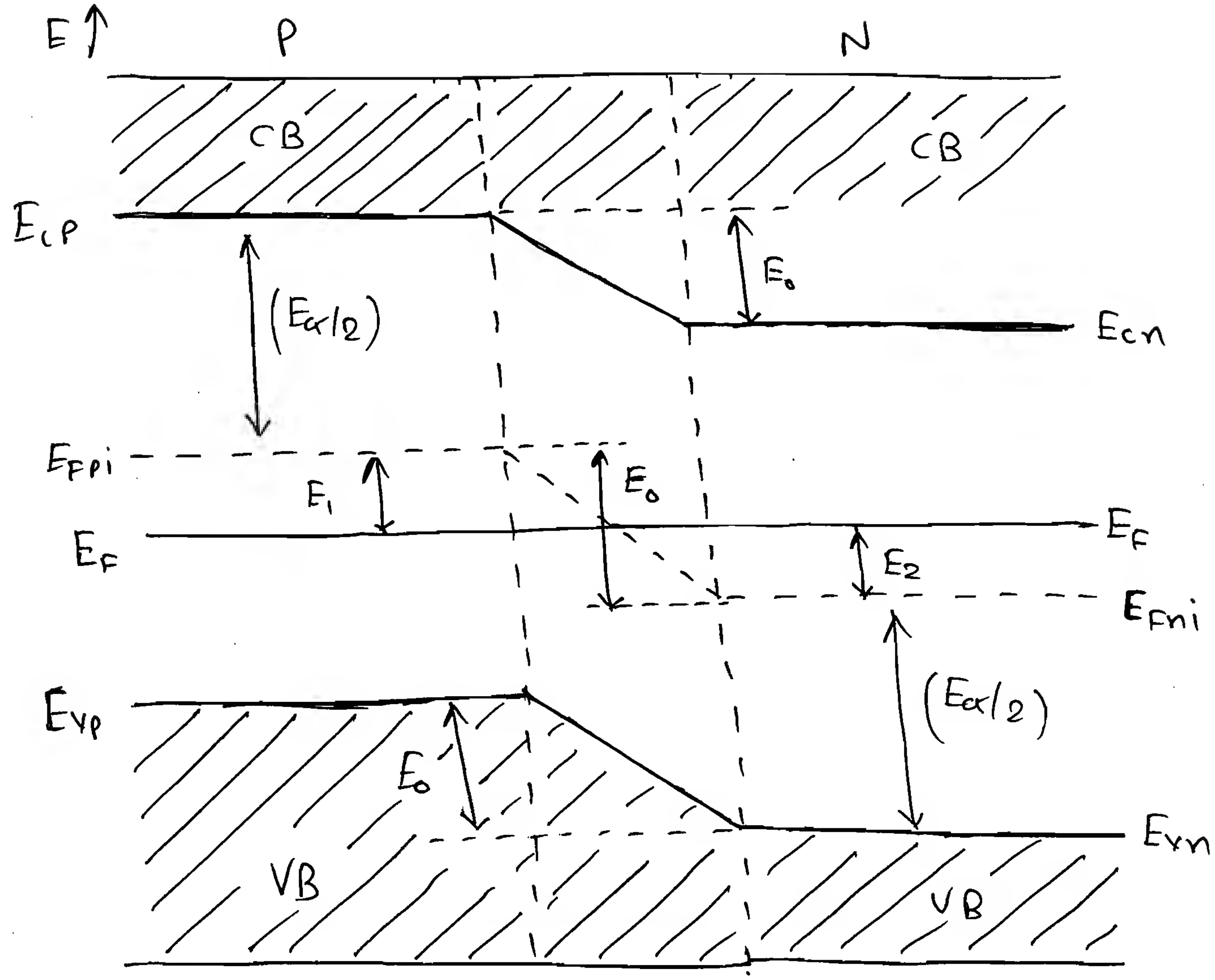
⇒ Fermi level is constant throughout the length of open circuited P-N diode.

⇒ Fermi level constant for an open circuited P-N Diode is valid at any P-N junction of any electronic device it is not constant for Forward biased (OR) Reverse biased.

⇒ E_0 (electron volts) (eV). is defined as shift between edges of conduction band and valance band of P & N sides.

⇒ V_0 (V) & E_0 (eV) (OR) Numerically equivalent

$$\boxed{\begin{aligned} E_0\,(eV) &= E_1 + E_2 = KT \ln\left(N_D N_A / n_i^2\right). \\ &= E_{cp} - E_{cn} = E_{vp} - E_{vn}. \end{aligned}}$$

⇒ 

⇒ Using eqn- (11) & (12) of fermi level discussion.

$$\boxed{\begin{aligned} E_1 &= KT \ln (N_A/n_i) \\ E_2 &= KT \ln (N_D/n_i). \end{aligned}}$$

Q For a germenium diode calculate fermi-level position in p-region. w.r.t. intrinsic fermi level. given,

$N_D = 10^{16}\ cm^{-3}$

$N_A = 3 \times 10^{18}\ cm^{-3}$.

$n_i = 2.5 \times 10^{13}\ cm^{-3}$.

Solⁿ:

$$E_1 = kT \ln (N_A / n_i).$$

$$\therefore E_1 = 0.026 \ln \left(\frac{3 \times 10^{18}}{2.5 \times 10^{13}} \right).$$

$$\boxed{E_1 = 0.304 \text{ eV}.}$$

[a] In a P-N diode width of depletion region under open ckt condⁿ is 0.334 µm. Calculate penetration of depletion region into P-side and E_0 & electric field intensity given

$$N_D = 10^{16} \text{ cm}^{-3}.$$

$$N_A = 4 \times 10^{18} \text{ cm}^{-3}.$$

$$\epsilon = 104.93 \times 10^{-14} \text{ F/m}.$$

Solⁿ:

$$x_{po} = \frac{W \cdot N_D}{N_D + N_A}.$$

$$\therefore x_{po} = \frac{0.334 \times 10^{-6} \times 100 \times 10^{16}}{10^{16} + 400 \times 10^{16}}$$

$$x_{po} = 0.0833 \times 10^{-6}$$

$$\therefore x_{po} = 0.0833 \times 10^{-6}$$

$$\boxed{x_{po} = 8.33 \times 10^{-8} \text{ cm}.}$$

$$\Rightarrow E_0 = -\frac{q \cdot N_A \cdot x_{po}}{\epsilon}$$

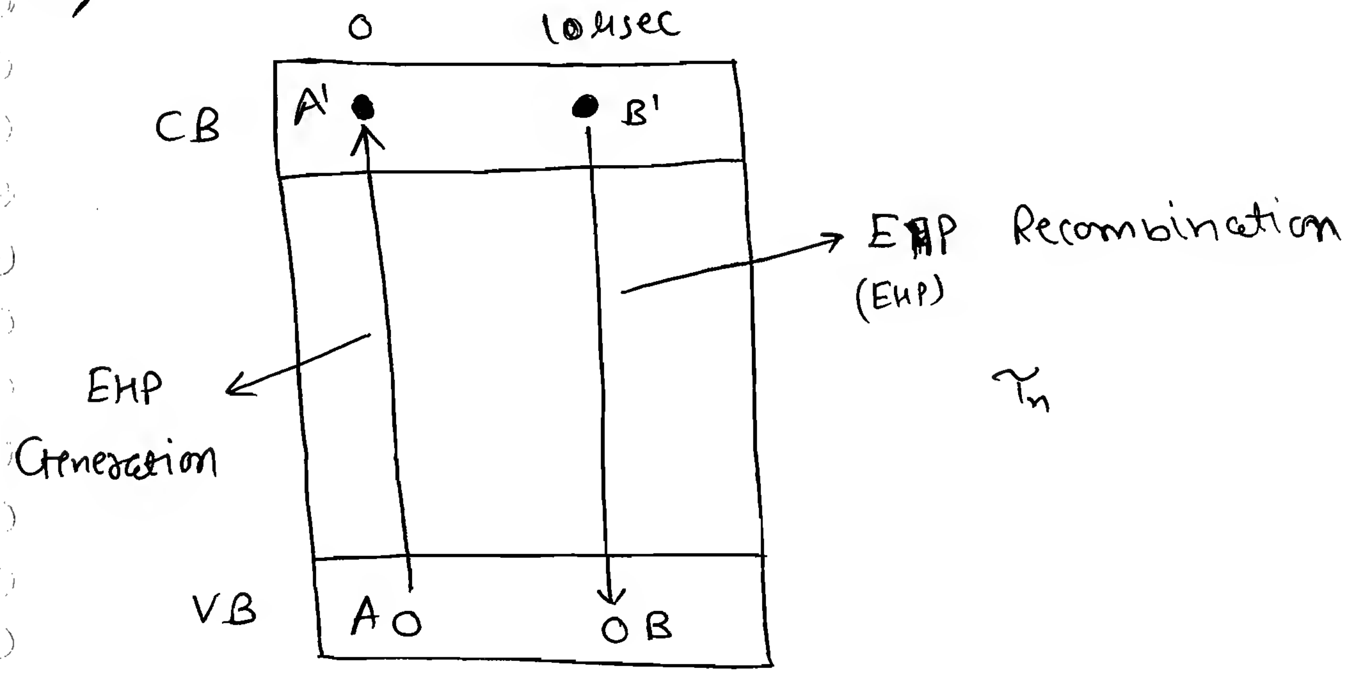
$$= \frac{-1.6 \times 10^{-19} \times 4 \times 10^{18} \times 8.33 \times 10^{-8}}{104.93 \times 10^{-14}}$$

$\therefore E_0 = -0.5 \times 10^5 \ eV/cm.$

$\therefore \boxed{E_0 = -50 \ kV/cm.}$

* Generation and Recombination of Charge Carriers :

⇒



⇒ During EHP generation a bound e^- becomes free and a hole is created both of them support current.

⇒ During EHP recombination one free e^- becomes bound and one hole disappears hence current decreases.

⇒ Life-time for e^-, hole τ_n, τ_p is defined as duration of time during which an e^-, hole support current

⇒ Diffussion length for $\bar{e}$, hole L_n, L_p is defined as distance travelled by an $\bar{e}$, hole during their corresponding life times given by L_n, =

$$\boxed{L_n = \sqrt{D_n T_n}}$$

&

$$\boxed{L_p = \sqrt{D_p T_p}}.$$

* Variation of minority Carrier concentration.

⇒ P_{no} : Initial thermally generated minority carrier concentration.

⇒ $P_n'(t)$, $P_n'(x)$: excess hole concentration at any time t, distance x generated due to illumination. (light rays).

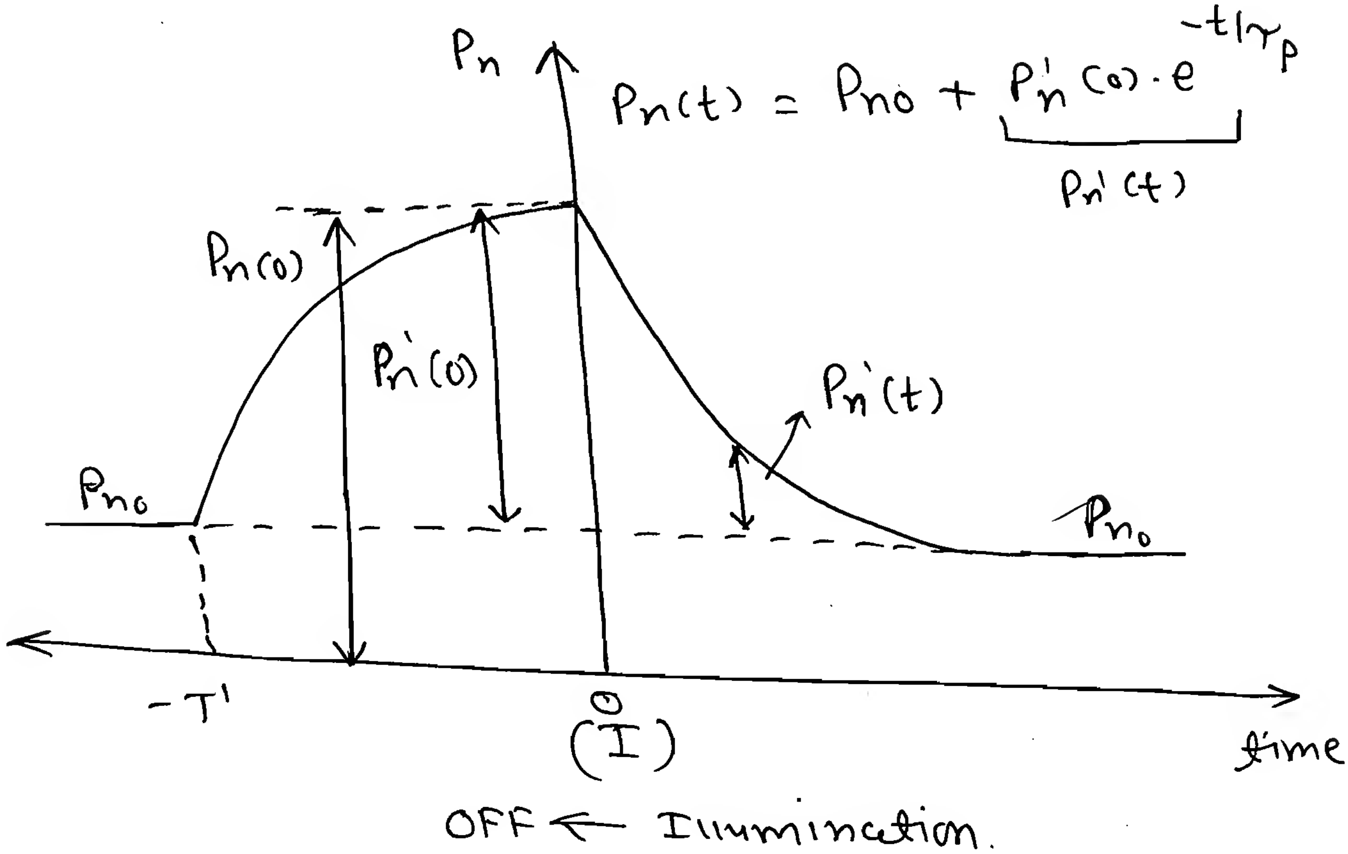
⇒ $P_n(t)$, $P_n(x)$: total hole concentration at any time t, distance x.

⇒ In fig - Ⓐ & Ⓑ, an n-type semiconductor is considered in which due to room

temp. EHP generation has occurred and P_{no} holes are generated.

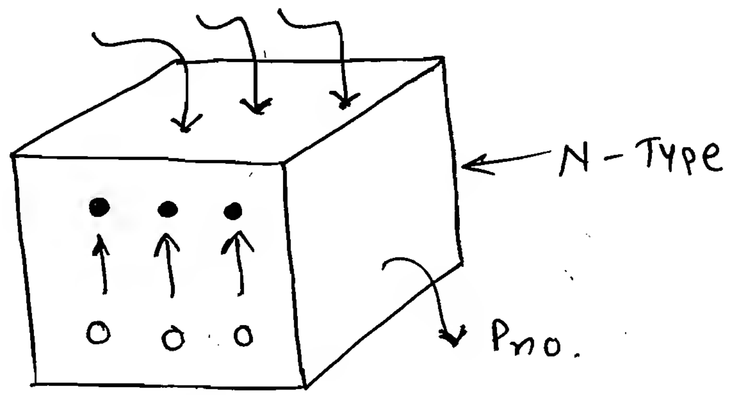
⇒ Fig-(A) :- with time:

→



(I)

→



(II)

→ ON to a n-type semiconductor having P_{no} holes. Some illumination is allowed to fall uniformaly starting from a time of $-T'$ due to which again EHP

generation occurs and again holes are generated which get added to P_{no}. ~~and~~ hence hole concentration increases.

→ At a time of 0 sec, illumination is switched off. A hole recombine after τ_p sec. Hence hole concentration decreases.

→ A hole generated due to illumination once recombine can not regenerate because illumination is switched off. whereas a hole generated due to room temp. after recombination regenerates since temp. is in on condition. Hence decreases in concentration stops at P_{no}.

$$P_n(t) = P_{no} + P_n'(0)\, e^{-t/\tau_p}$$

$$t=0: \quad P_n(0) = P_{no} + P_n'(0) \cdot e^{-0} = P_{no} + P_n'(0).$$

$$t=\infty: \quad P_n(\infty) = P_{no} + P_n'(0) \cdot e^{-\infty} = P_{no}.$$

→ % increase in minority carrier concentration due to illumination is very much greater than % increase in majority carrier

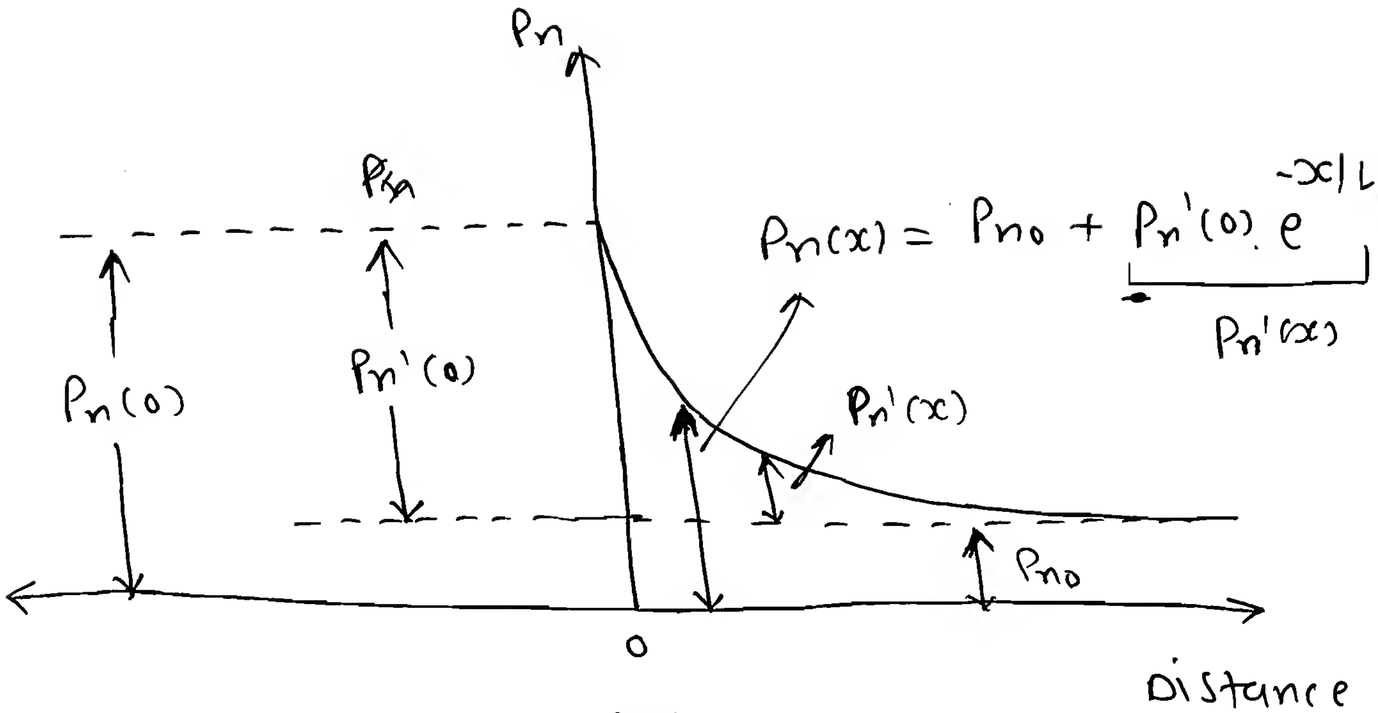
concentration.

N-Type:

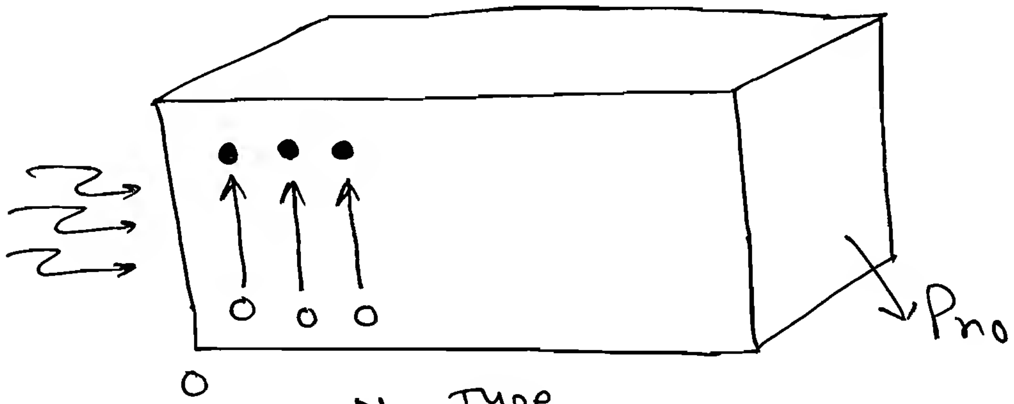
	I.I.	(Temp.) B.B.		(Illumi.) B.B.
e^- :	100	10	$\xrightarrow{9\%}$	10
Hole :	—	10	$\xrightarrow[100\%]{}$	10

⇒ **Fig- (B) With distance:**

⇒ ON to an n-type semiconductor having P_{no} holes some illumination is allow to fall only at left side. Centered at distance zero. and matches with origin. Due to which again EHP generation occurs and again holes are generated which get added to P_{no}. Hence hole concentration increases to left side. due to difference in concentration hole diffuse from higher to lower concentrated area. after travelling L_p distance a hole recombines hence hole concentration decreases.



(I).



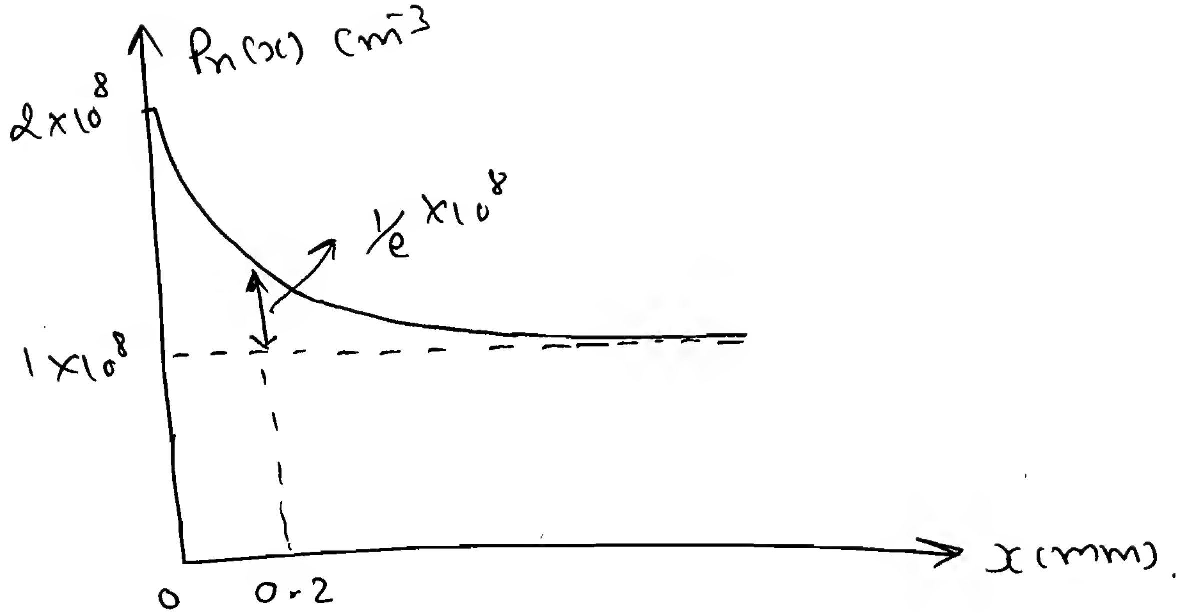
N - Type

(II)

Q An N-type silicon bar is illuminated at one end ($x = 0$). the minority Carriers Concentration variation is as shown given $n_i = 1.5 \times 10^{10}\ cm^{-3}$. calculate

(A) e^- Concentration.

(B) Diffussion length for holes.



Soln: (A) $n_{no} = n_i^2 / P_{no}$.

$$= \frac{(1.5\times10^{10})^2}{1\times10^8}$$

$$\boxed{n_{no} = 2.25 \times 10^{12} \ cm^{-3}.}$$

(B) $L_p = ?$

$$P_n'(x) = P_n'(0)\, e^{-x/L_p}.$$

~~assume~~ $x = 0.2mm$: $\frac{1}{e}\times10^8 = (2\times10^8 - 1\times10^8)\, e^{-0.2mm/L_p}$

$$\Rightarrow \boxed{L_p = 0.2mm.}$$

(c) What fraction drift current is due to electrons in pure germenium given

$\mu_n = 3800$ $cm^2/v\text{-}sec$

$\mu_p = 1800$ "

Soln: drift current $I = nq\mu_n EA + Pq\mu_p EA.$ — (2)

→ Pure germenium ⇒ Intrinsic

hence, $n = p = n_i$.

→ $$\frac{I_n}{I_n + I_p} \times 100 \quad \text{—— (1)}$$

→ substitude I_n and I_p from eqn- (2) into (1).

$$\frac{I_n \times 100}{I_n \times I_p} = \frac{n_i \cdot q \cdot \mu_n EA \times 100}{n_i q \mu_n EA + n_i q \mu_p EA}$$

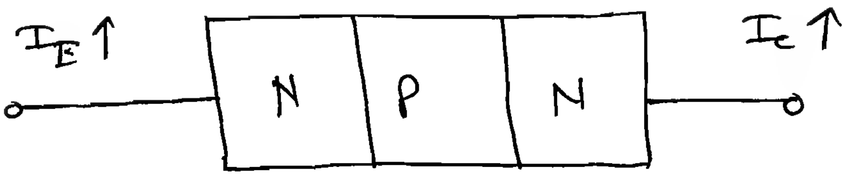
$$= \frac{\mu_n \times 100}{\mu_n + \mu_p}$$

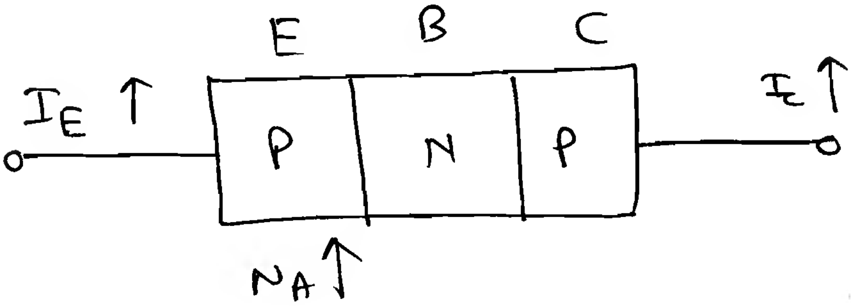
$$= \frac{3800}{3800 * 1800} \times 100$$

$$= \boxed{67.85\ \%}$$

Note:

→ For practical application N-type devices like n-p-n transistor, n-channel JFET, induced n-channel MOSFET etc are prefered over corresponding p-type devices, since n-type devices work-out cheaper.





$$\Rightarrow \quad I = \overset{\uparrow}{n q \mu_n E A} + p q \mu_p E A. \qquad \text{COST} \uparrow$$

$$I_{E(NPN)} > I_{E(PNP)}.$$

Q Calculate change in contact potential if dopping on n-side is increased by a factor of 1000 and dopping on p-side is unaffected.

Sol^n:

$$V_0 = KT \ln\left(\frac{N_A \cdot N_D}{n_i^2}\right)$$

$$V_0 = 0.026 \ln\left(\frac{N_A \cdot N_D}{n_i^2}\right).$$

$$\rightarrow V_{02} - V_{01} = KT \ln\left(\frac{N_{A2}\, N_{D2}}{n_i^2}\right) - KT \ln\left(\frac{N_{A1} \cdot N_{D1}}{n_i^2}\right).$$

$$= KT\left[\ln\left(N_{D2} \cdot N_{A2}/n_i^2\right) - \ln\left(\frac{N_{D1} \cdot N_{A1}}{n_i^2}\right)\right].$$

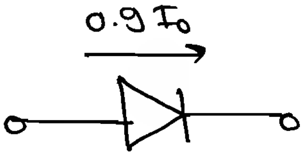
$$\therefore V_{02} - V_{01} = KT \ln \left(\frac{N_{D2} \cdot \cancel{N_{A2}}}{\cancel{n_i^2}} \times \frac{\cancel{n_i^2}}{N_{D1} \cdot \cancel{N_{A1}}} \right).$$

$$\therefore V_{02} - V_{01} = KT \ln \left(\frac{1000 \cancel{N_{D1}}}{\cancel{N_{D1}}} \right). \quad (\because N_{A1} = N_{A2}).$$

$$\therefore \boxed{V_{02} - V_{01} = 0.179 \text{ V}.}$$

Q. Calculate a voltage across a si diode if 90% reverse saturation current is flowing in forward bias.

Soln:



$$I = I_0 \left(e^{V/\eta V_T} - 1 \right).$$

$$\therefore 0.9 \cancel{I_0} = \cancel{I_0} \left(e^{V/2 \times 0.026} - 1 \right).$$

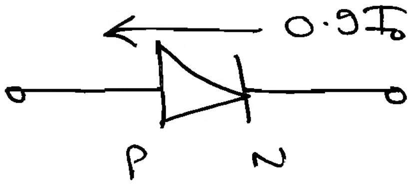
$$1.9 = e^{\frac{V}{0.052}}.$$

$$\therefore \boxed{V = 0.03337 \text{ V}}$$

$$\Rightarrow \boxed{V = 33.37 \text{ mV}}$$

Q. Find voltage at which reverse current in a Ge diode will reach 90% of its saturation value.

Soln:



$$\therefore \quad I = I_0 \left(e^{V/nV_T} - 1 \right).$$

$$\therefore \quad -0.9 \cancel{I_0} = \cancel{I_0} \left(e^{V/nV_T} - 1 \right).$$

$$\boxed{V = -59.86 \, mV}$$

__Note:__ while substituting a value for an entity, substitute along with sign while calculating the value of an entity dont disturb the existing sign.

☆ ZENER DIODE:

→ V_Z : Knee (or) breakdown Voltage.

$I_{Z(min)}$: Knee (or) minimum current.

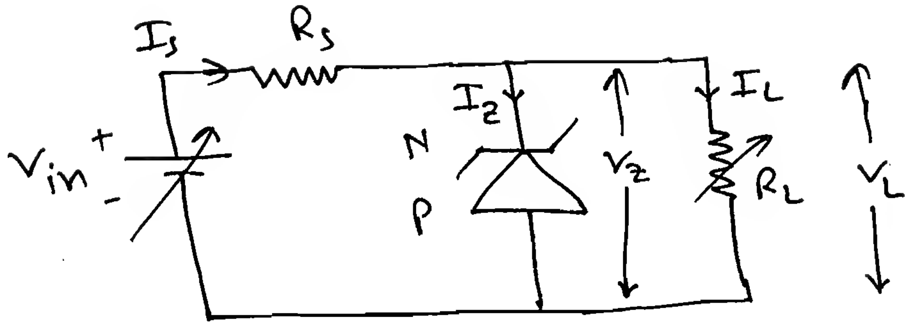
R_Z : dynamic reverse breakdown Resistance.

NBO : Non breakdown.

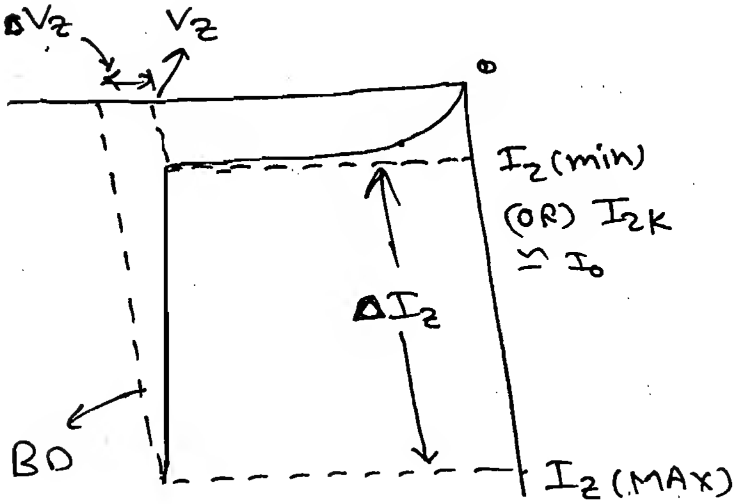
→ Zener diode is named after its inventor C. Zener. In the ckt symbol, z differentiates zener diode from PN diode. The direction of arrow shows the direction of flow of current when the diode is forward bias. PN, zener and Tunnel diodes are two terminal devices, Identical in Construction with only difference in doping concentration.

→ In PN 1 IN 10^8, In zener 1 In 10^5 and In Tunnel 1 IN 10^3. the forward and Reverse charac. of zener diode are identical to forward and reverse char. of PN diode except that zener diode can be operated in Revers BD whereas P-N diode should not be operated in Reverse B.D.

⇒

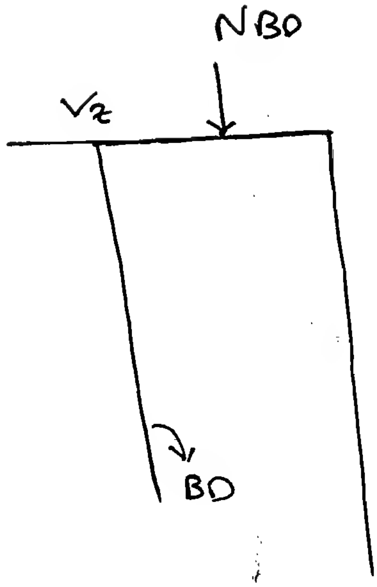


⇒



Practical

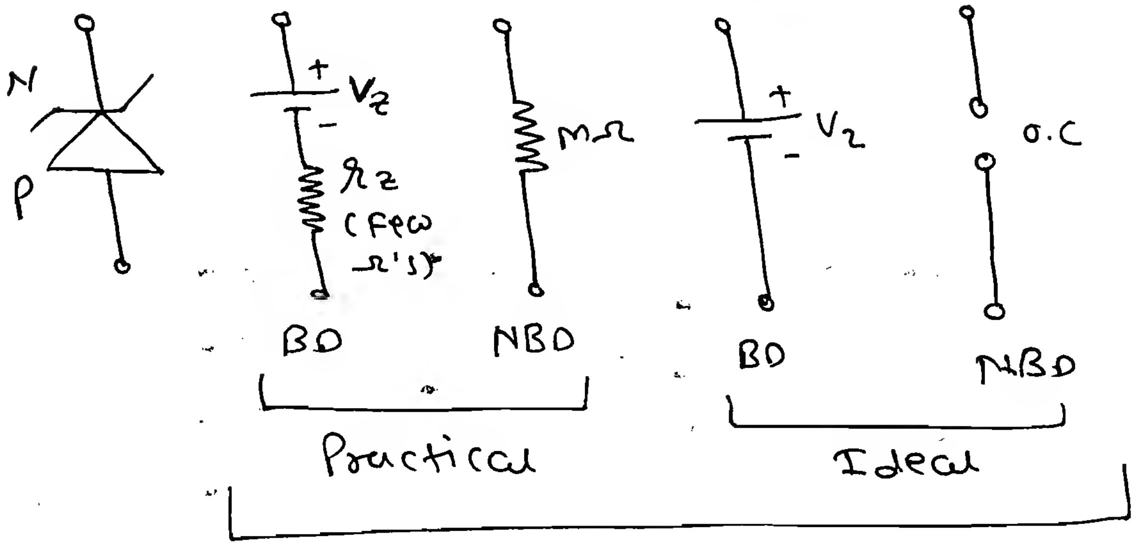
$r_Z = \Delta V_Z / \Delta I_Z$



Ideal

$r_Z = 0.$

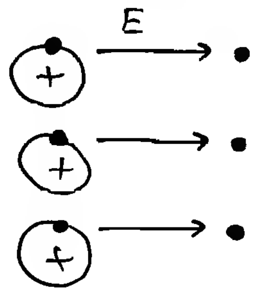
⇒



Equivalent circuits.

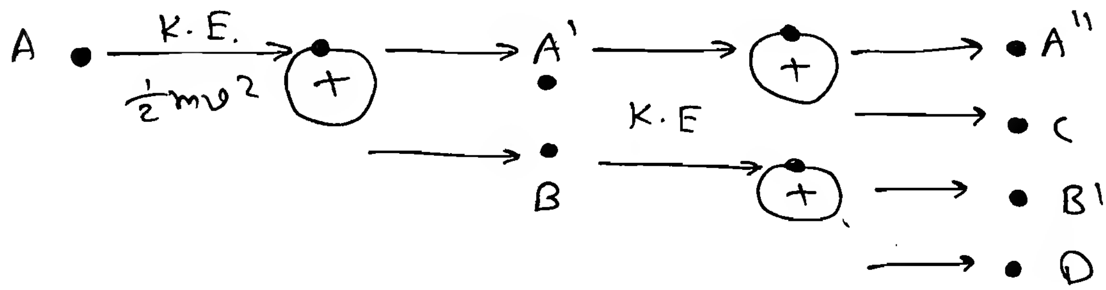
⇒ <u>Zener</u> <u>Breakdown:</u>

→ Due to applied reverse biased a large electric field gets developed across Zener diode which pulls out charge carrier by breaking covelent bonds and making atoms ions called field ionization. Vouminus charge carrier thus generated are responsible for large current. This breakdown occurs in relatively more dopped step junction diodes at $V_z < 6V$ with $\frac{dV_z}{dt} = -0.1\ \%/^\circ C$



⇒ <u>Avalanch</u> <u>Break down:</u>

→ ~~Ion~~



⇒ $1 \rightarrow 2 \rightarrow 4 \rightarrow 8 \rightarrow 16 \rightarrow \ldots$

Carrier Multiplication. → Impact Ionization.

Avalanch Multiplication.

→ A thermally generated charge carrier gets attracted towards opposite polarities of applied reverse biased gain kinetic energy and collieds with an atom on the way and transfer its kinetic energy to a valance shell electron of the atom and push that electron to conduction band and makes it free thus one free carrier becomes two. The process repeate further and due to carrier (or) avalanch multipiication voluminus carriers are generated which are responsible for large current. Due to collission an atom becomes ion called Imapcet Ionization.

This breakdown occurs in relatively less dopped linear junction diodes at $V_Z > 6V$. with $\frac{dV_Z}{dT} = +0.1\ \%/^\circ C$.

⇒ In the above equivalent ckt, +ve of V_Z should matched with n-side of diode.

⇒ The above equivalent ckt are valid only for reversed biased zener

diode. for a forward bias zener diode use any of the three forward biased eqn ckt of P-N Diode.

* **Voltage Regulator:**

⇒ A Voltage regulator should maintain constant voltage across terminals of load irrespective of fluctuation in load (or) supply.

⇒ A Zener diode can ~~act~~ act as voltage regulator if it is operated in reverse breakdown for which the following condition to be satisfied.

(i) Current through zener diode should be greater than (or) equal to I_{zmin}.

(ii) Voltage across terminals of zener diode should be V_z, BD Voltage.

⇒ **Fixed Input Variable load:**

R_L : $I_{s(fix)} = I_z + I_L$: $V_L = I_L \cdot R_L$

R_L : $I_{s(fix)} = I_z \uparrow + I_L \downarrow$: $V_L = (I_L \downarrow) \cdot (R \uparrow)$

R_L :

$\Rightarrow$

$R_L : I_{S(fix)} = I_Z + I_L : V_L = I_L \cdot R_L$

$R_L \uparrow : I_{S(fix)} = I_Z \uparrow + I_L \downarrow : V_L = (I_L \downarrow)(R_L \uparrow)$

$: \underline{I_Z < I_{Z(max)}}$.

$R_L \downarrow : I_{S(fix)} = I_Z \downarrow + I_L \uparrow : V_L = (I_L \uparrow)(R_L \downarrow)$

$: \underline{I_Z \geq I_{Z(min)}}$.

$\Rightarrow$ Vin is fixed, R_L can vary hence I_S is fixed.

$\rightarrow$ For a given R_L, $I_{L(fix)} = I_Z + I_L$ with $V_L = I_L \cdot R_L$. say R_L increases then I_L decreases. hence I_Z increases by equal amount since I_S is fixed.

$\rightarrow$ Though I_L increases, Voltage across ideal zener in breakdown, V_Z is Constant hence $V_L = V_Z$ is constant (or) increased R_L and decreased I_L Counter each other to make $\underline{V_L = I_L . R_L}$ <u>Constant.</u>

⇒ <u>Variable input fixed load:</u>

→ $V_{in}: I_s = I_z + I_{L(fix)}$: $V_L = I_L \cdot R_L$.

$V_{in}\uparrow : I_s\uparrow = I_z\uparrow + I_{L(fix)}$: $V_L = I_L \cdot R_L$

: $I_z < I_{z(max)}$.

$V_{in}\downarrow : I_s\downarrow = I_z\downarrow + I_{L(fix)}$: $V_L = I_L \cdot R_L$.

: $I_z \geq I_{z(min)}$.

⇒ V_{in} can vary & R_L is fixed. hence I_L is fixed.

→ For a given R_L, $I_s = I_z + I_{L(fix)}$ with $V_L = I_L \cdot R_L$. Say V_{in} increases then I_s increases hence I_z increases by equal amount making I_L fixed. Current always prefers least resistive path and resistance of ideal zener in BD is zero.

→ Though I_z increases voltage across ideal zener in break down V_z is constant. Hence $V_L = V_z$ is constant

(or) since I_L & R_L are fixed,

$V_L = I_L \cdot R_L$. is constant.

* Procedure to Solve Numericals: Imp.

(i) Identify whether Zener diode is ideal (OR) Practical.

(ii) If the diode is FB replace by any of the three FB equivalent Ckt of P-N Diode.

(iii) If the diode is reverse biased verify BD status and replace by appropriate equivalent Ckt.

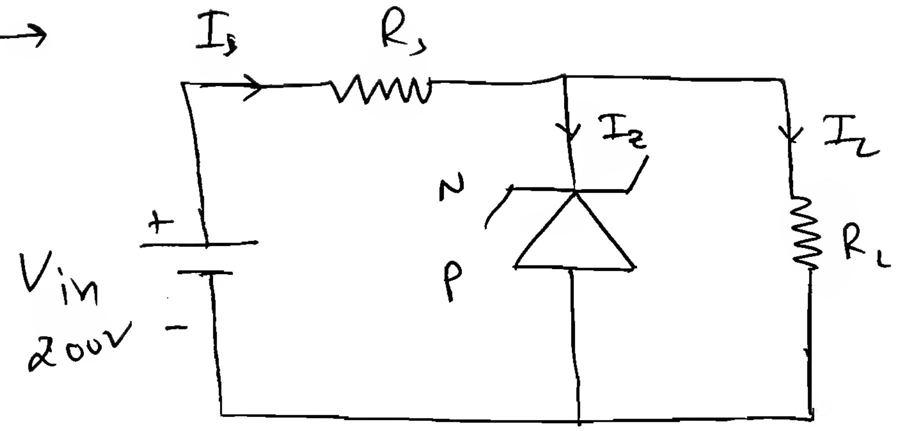
(iv) Apply KCL (OR) KVL.

Q. A 50 V, 5 to 40 mA Zener diode is used as shown in a regulator Ckt

(A) Calculate R_s to allow Voltage regulation from $I_L = 0$ to I_{Lmax}. also calculate I_{Lmax}.

(B) If R_s is set as found in Part-(A) and I_L is fixed at 25mA find the permissible range of V_{in} for Zener diode to act as regulator safely.

→



Soln:

given data:

→ $V_z = 50V$.

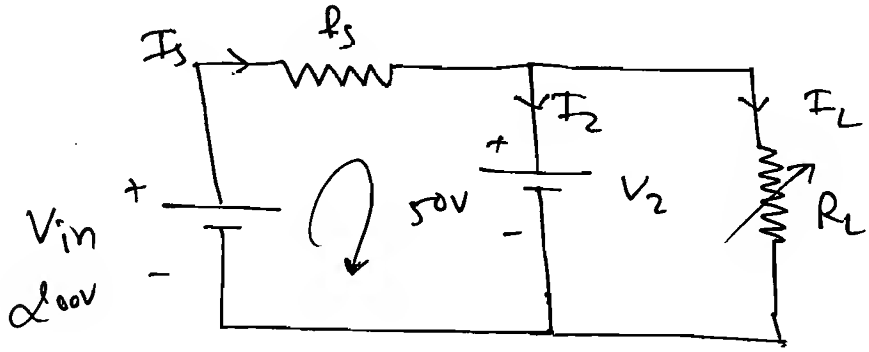
$I_{z(min)} = 5mA$.

$I_{z(max)} = 40mA$.

$R_z = 0\ \Omega$
↓
Ideal.

(A) Fixed input Variable load.

→ zener diode is in BD. replace with by its eqn ckt. (voltage source V_z).



→ $I_{s(fix)} = I_{z(max)} + I_{L(min)}$

$= 40 + 0 = 40mA$.

By KVL, $200 = I_s \cdot R_s + 50$

$V_{in} = I_{s(fix)} \cdot R_s + V_z$.

$$\Rightarrow R_S = \frac{(200-50)}{40mA} = 3.75\,k\Omega$$

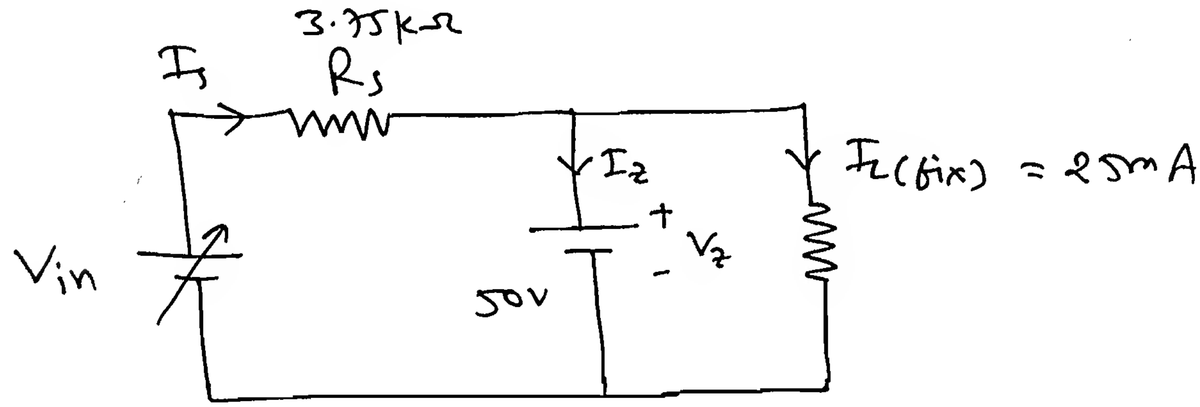
$$\boxed{R_S = 3.75\,k\Omega}$$

$$\Rightarrow I_{S(fix)} = I_{Z(min)} + I_{L(max)}.$$

$$\therefore 40 = (5) + I_{L(max)}$$

$$\Rightarrow \boxed{I_{L(max)} = 35mA}$$

(B) <u>Variable</u> <u>input</u> <u>fixed</u> <u>load:</u>



$$\Rightarrow I_{S(min)} = I_{Z(min)} + I_{L(fix)}$$
$$= 5mA + 25mA = 30\,mA.$$

$$\Rightarrow I_{S(max)} = I_{Z(max)} + I_{L(fix)}$$
$$= 40 + 25 = 65\,mA.$$

$$\therefore V_{in(min)} = I_{S(min)} \cdot R_S + V_Z.$$

$$V_{in(min)} = (30 \times 3.75) + 50$$

$$V_{in(min)} = 162.5\,V$$

$\therefore \; V_{in(max)} = (65 \times 3.75) + 50.$

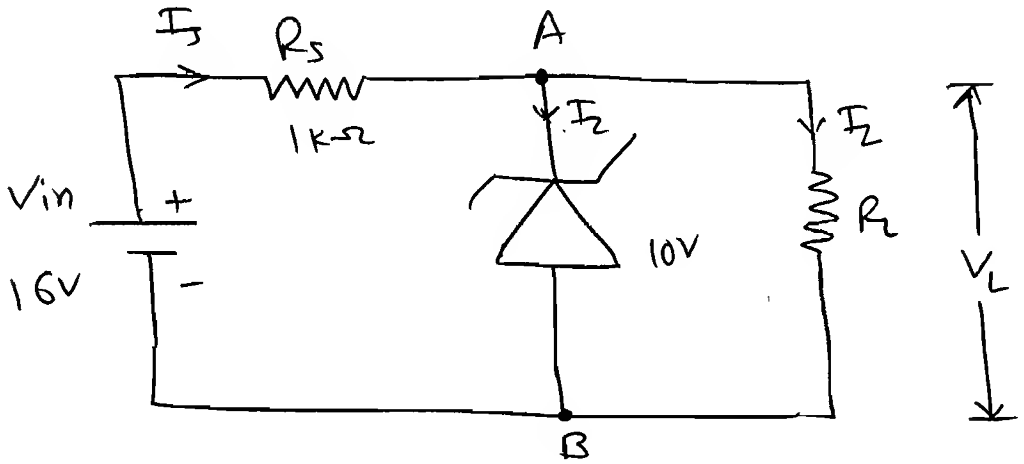
$$\boxed{V_{in(max)} = 293.75\,V}$$

So, range of Vin is $162.5\,V$ to $293.75\,V$.

[Q] For the given Zener diode ckt. Calculate V_L given

(A) $R_L = 1.2K\,\Omega$

(B) $R_L = 3\,K\,\Omega$



Sol^n:

$I_{Z(min)} = 0, \quad r_Z = 0$

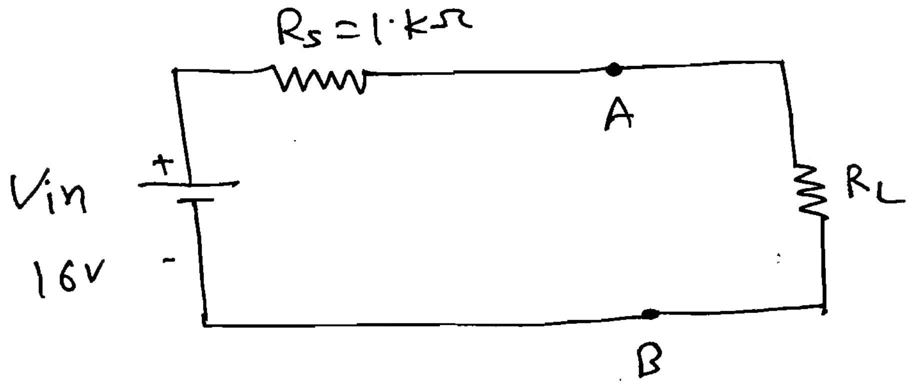
$V_Z = 10V$

for a Zener diode to go into BD the following two Conditions are to be satisfied.

(1) Current through Zener diode Should be greater than (or) equal to $I_{Z(min)}$ which is already satisfied

since $I_{z(min)} = 0$.

(2) Voltage across terminals of Zener diode should be V_z, BD voltage. To verify this physically remove Zener diode from ckt and measure V_{AB} as shown.



$$V_{AB} = \frac{R_L \times 16}{R_L + R_s}.$$

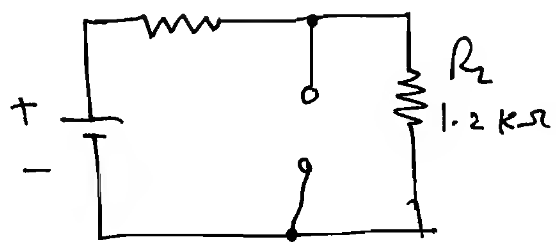
$$\therefore V_{AB} = \frac{16 \times R_L}{1K + R_L}.$$

(A) $R_L = 1.2\,K$

$V_{AB} = 8.73\,V.$

→ Zener diode is not in BD replace it by its equivalent, o.c.

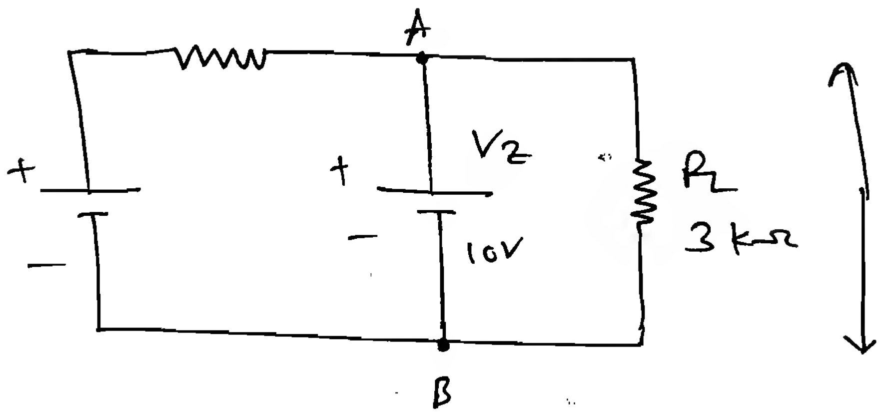
$$\boxed{V_L = V_{AB} = 8.73\,V}$$



(B) $R_L = 3k$

→ $\boxed{V_{AB} = 12V}$

→ Zener diode is in BD. replace it by its equivalent, Voltage source V_Z



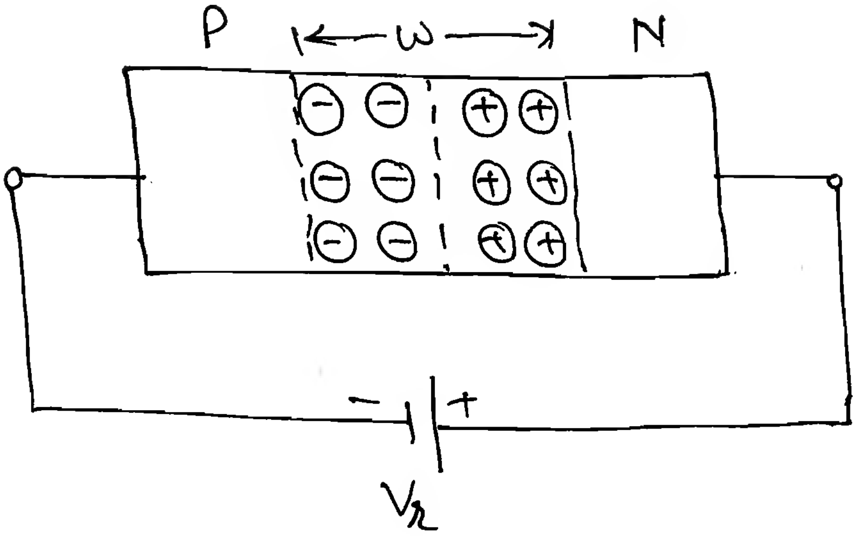
$\boxed{V_L = 10V}$

* Transition region (or) Depletion region (or) Space charge region (or) Barrier Capacitance C_T :

⇒ Change in reverse bias changes in depletion width and ions of depletion region. Hence a non-zero value of $\frac{dq}{dt}$ is exibuted by depletion region which is by defination Capacitance Called depletion region Capacitance.

⇒ $C_T = \epsilon A / W$.

⇒



⇒ ω is proportional to $V_j^{1/2}$

⇒ $\omega \propto V_j^{1/2}$ for step (or) abrupt j^n.

⇒ $\omega \propto V_j^{1/3}$ for linear (or) graded j^n.

where, j^n voltage. $V_j = V_0 - V_d$.

where, V_0 : open circuited contact potential.

& V_d : Voltage across diode.

(V_d is -ve for RB).

$$\therefore \boxed{C_T = \sqrt{\frac{q \epsilon A^2}{2\left(\frac{1}{N_D} + \frac{1}{N_A}\right)(V_0 - V_d)}}}$$

→ Transition capacitance at zero bias,

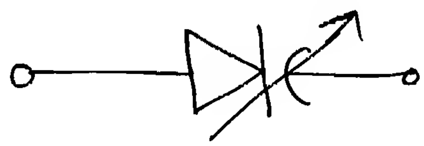
$$C_{T_0} = C_T\big|_{V_d = 0}$$

$$\rightarrow \boxed{C_T = \frac{C_{T0}}{\left(1 - \frac{V_d}{V_0}\right)^{m_T}}}$$

$m_T = 0.5$ for step junction. &

$= 0.33$ for linear "

⇒ Change in reverse bias changes width of depletion region and capacitance. Hence it can be used as voltage variable capacitor (or) Varicap. (or) Varactor diode:



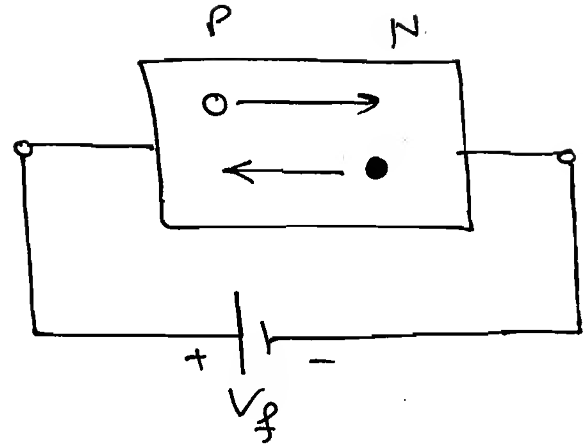
* Diffussion Capacitance:

⇒ Change in forward bias changes magnitude of diffussing charges and current. Hence, a non-zero value of $\frac{dI}{dV}$ is exibitted by diffussing charges which is by defination capacitance called Diffussion Capacitance.

$$\boxed{C_D = \frac{\tau I}{\eta V_T}}$$

where, $\tau = \tau_p + \tau_n$.

⇒



$\frac{dQ}{dx} \neq 0.$

$$\boxed{C_D = \frac{\tau I}{\eta V_T}}$$

Where, $\tau = \tau_p + \tau_n$.

Q A silicon diode has a diffussion Capacitance of $1\,\mu F$ when carrying a Current of $1 mA$. Assumming $N_A \gg N_D$. Calculate τ_p.

Soln: $N_A \gg N_D$, hence C_D eqn gets modified to

$$C_{DP} = \frac{\tau_p \cdot I}{\eta V_T}.$$

$$\tau_p = \frac{1 \times 10^{-6} \times 2 \times 0.026}{1 \times 10^{-3}}$$

$$\boxed{\tau_p = 52\,\mu s}$$

Q A Step junction si diode with $V_0 = 0.637 V$ has transition Capacitance at zero bias as $0.5 PF$. Calculate C_T at the reverse

of 5 V.

Sol^n: Here, $C_{T0} = 0.5\ PF$

$$C_T = \frac{C_{T0}}{\left(1 - \frac{V_a}{V_0}\right)^{m_T}}$$

$$= \frac{0.5 \times 10^{-12}}{\left(1 - \frac{(-5V)}{0.637}\right)^{0.5}}$$

$$\therefore \boxed{C_T = 0.168\ PF}$$

Q A reverse biased diode is having a junction Voltage of 8V and junction Capacitance 15 PF. If junction voltage is increase to 12V Capacitance drops to 13.5 PF find wheter it is abrupt (or) graded junction.

Sol^n: Assumption: Abrupt junction.

$\omega \propto V_j^{1/2}$, ϵ & A are constant

hence $C_T \propto \frac{1}{V_j^{1/2}}$.

$$\therefore \frac{C_{T2}}{C_{T1}} = \left(\frac{V_{j1}}{V_{j2}}\right)^{1/2}$$

$$\therefore \frac{C_{T2}}{C_{T1}} = \left(\frac{8}{12}\right)^{1/2} =$$

$$\therefore C_{T_2} = 0.82 \times C_{T1}$$

$$C_{T_2} = 12.25 \text{ PF}.$$

→ C_{T_2} is not equal to 13.5 PF. hence it is not abrupt i.e. it is graded junction.

* Effect of Temperature on Reverse Saturation Current I_o.

⇒ Increase in temp. increases EHP generation and minory concentration hence I_o increases i.e. $\frac{dI_o}{dt} > 0$.

$$\therefore \boxed{I_o = \frac{Aq D_p p_{no}}{L_p} + \frac{Aq D_n n_{po}}{L_n}}.$$

⇒ From the above eqn after analysis we get,

$$\Rightarrow \boxed{\frac{1}{I_o}\cdot\frac{dI_o}{dt} = \frac{m}{T} + \frac{E_{go}}{\eta T V_T}}$$

Where, $m = 1.5$ for Si
$= 2$ for Ge.

$$\left.\begin{aligned}\frac{1}{I_o}\cdot\frac{dI_o}{dt} &= 8\ \%/^\circ C \text{ for Si}\\ &= 11\ \%/^\circ C \text{ for Ge}\end{aligned}\right] \text{At } 300^\circ K.$$

⇒ Practically for both diodes rise is found to be $7\ \%/^\circ C$.

⇒ I_o gets doubled for every $10^\circ C$ rise temp. i.e.

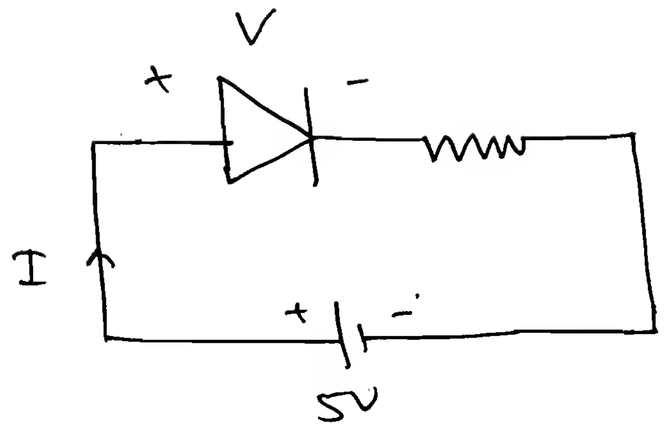
$\cancel{I_{o2} = I_{o1}}$

$$\boxed{I_{o2} = I_{o1}\cdot 2^{(T_2 - T_1)/10}}$$

* Effect Temp. on Voltage:

⇒ For $1^\circ C$ rise in temp. to maintain Constant Current through diode decrease Voltage across diode by 2.5 mV i.e. $\boxed{\frac{dV}{dT} = -2.5\ mV/^\circ C}$

⇒



$$\boxed{I = I_0 \left(e^{V/\eta V_T} - 1\right)}$$

⇒ From current eqn of diode after analysis we get,

$$\boxed{\frac{dV}{dT} = \frac{V - (E_{G0} + m\eta V_T)}{T}}$$

$= -2.1\ mV/°C \rightarrow Ge$ } At 300°K.

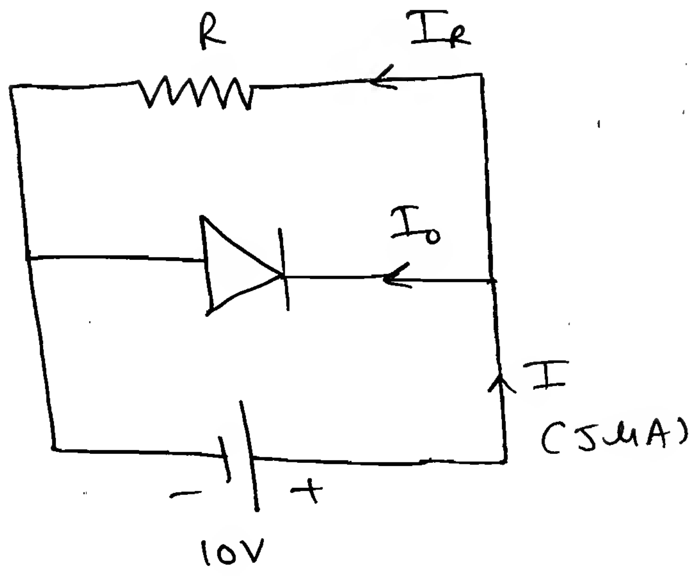
$= -2.3\ mV/°C \rightarrow Si$

<u>Note:</u>

⇒ The above value of $\frac{dV}{dT}$ is valid only for forward bias.

$\boxed{Q}$ The current I of circuit was found to be increasing by 7 %/°C rise in temp. Calculate I_0 assuming Ge diodes reverse sat. currents temp co-efficient is 11 %/°C.

$\Rightarrow$



Sol^n: given data,

$$\frac{1}{I}\cdot\frac{dI}{dt} = 7\ \%/^\circ C$$

$$\frac{1}{I_o}\cdot\frac{dI_o}{dt} = 11\ \%/^\circ C$$

By, KCL $\quad I = I_o + I_R.$

$$\frac{dI}{dt} = \frac{dI_o}{dt} + \cancel{\frac{dI_R}{dt}}^{\,0}. \quad (\because R = \text{const}^n \Rightarrow I_R = \text{const}^n).$$

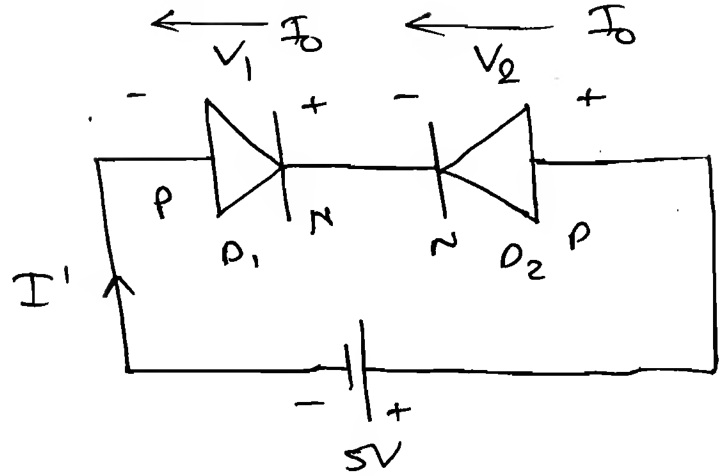
$$\therefore \underset{5\mu A}{I}\underbrace{\left(\frac{1}{I}\cdot\frac{dI}{dt}\right)}_{0.07} = I_o\underbrace{\left(\frac{1}{I_o}\cdot\frac{dI_o}{dt}\right)}_{0.11}.$$

$$\therefore I_o = \frac{5\times 0.07}{0.11}$$

$$\therefore \boxed{I_o = 3.18\,\mu A.}$$

(a) Two Ge diode connected as shown.

Calculate V_1, V_2 & I'.



Soln:

$\boxed{D_2}$: $I = I_0 \left(e^{V/\eta V_T} - 1\right)$.

$\therefore \; I_0 = I_0 \left(e^{\frac{V}{\eta V_T}} - 1\right)$.

$\therefore \; 2 = \cancel{x} \; e^{V/\eta V_T}$

$V = \boxed{18 \cdot mV. = V_2.}$

By KVL, $\quad 5 = V_1 + V_2.$

$\therefore \; V_1 = 5 - V_2$

$\therefore \; \boxed{V_1 = +4.982}$

Note: → While giving answer for a Voltage consider the polarities given in problem statement.

→ While giving answer for a current consider the direction shown in prob. statement.

$\rightarrow \quad \boxed{I' = -I_0}$

Q The reverse saturation current density of a Ge diode is 1 mA/m². Find the voltage to be applied across it in forward bias to get a current density of 10^5 mA/m².

Soln: divide $I = I_0(e^{V/nV_T} - 1)$ by cross-sectional area A,

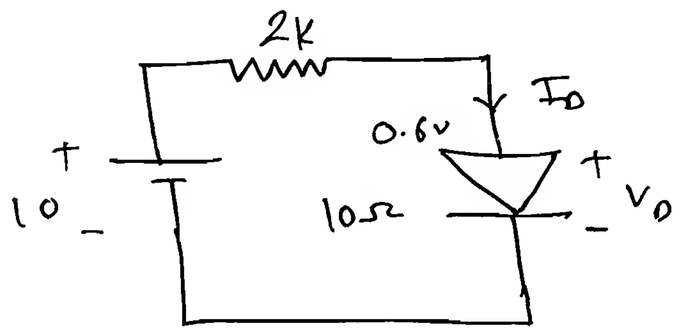
$$\therefore \frac{I}{A} = \frac{I_0}{A}\left(e^{\frac{V}{nV_T}} - 1\right).$$

$$\Rightarrow \boxed{J = J_0\left(e^{\frac{V}{nV_T}} - 1\right).}$$

$$\therefore 10^5 = 1\left(e^{\frac{V}{1\times 0.026}} - 1\right).$$

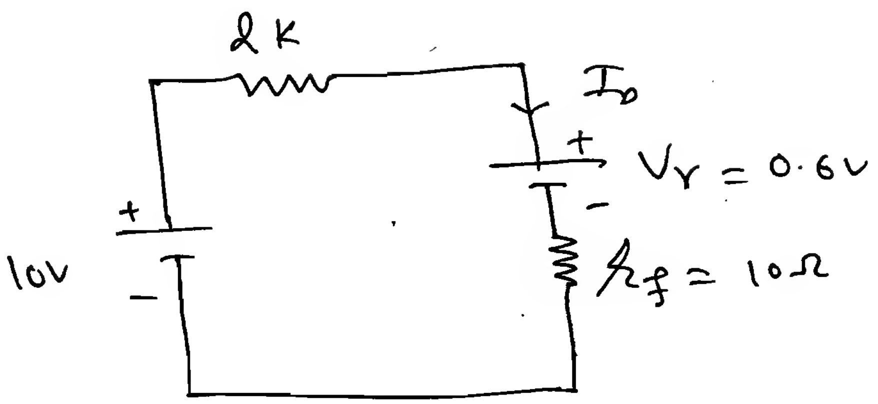
$$\therefore \boxed{V = 0.3\text{ V.}}$$

Q



Calculate I_D & V_o in the given ckt.

Sol^n:



$$I_D = \frac{10 - 0.6}{2K + 10} = 4.67\,mA.$$

$$\therefore \boxed{I_D = 4.67\,mA.}$$

$$\therefore V_D = V_\gamma + I_D \cdot R_f$$

$$= 0.6 + (4.67 \times 10^{-3} \times 10)$$

$$\therefore \boxed{V_D = 0.646.\,V}$$

☆ Tunnel (Esaki) Diode:

→ $E_{Fn} = E_c - KT \ln (N_c / N_D)$.

$E_{FP} = E_V + KT \ln (N_V / N_A)$.

$E_G = KT \ln (N_c \cdot N_V / n_i^2)$.

$E_0 = KT \ln (N_D \cdot N_A / n_i^2)$.

⇒ **Heavy Dopping:** (Tunnel)

$N_D > N_C$
$N_A > N_V$

$E_{Fn} > E_C$

$E_{FP} < E_V$

$E_0 > E_G$

Normal Doping: (PN).

$N_C > N_D$
$N_V > N_A$

$E_{Fn} < E_C$

$E_{FP} > E_V$

$E_G > E_0$

⇒

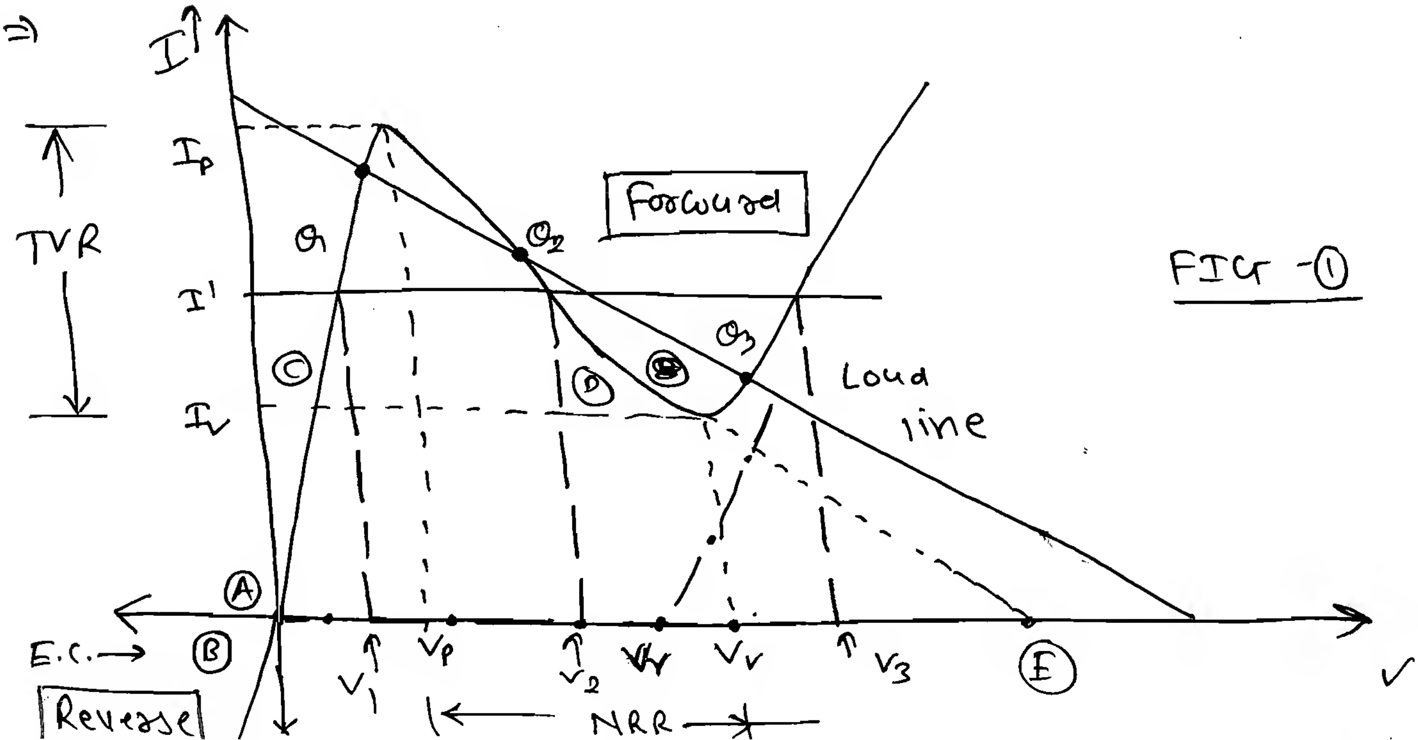


FIG - ①

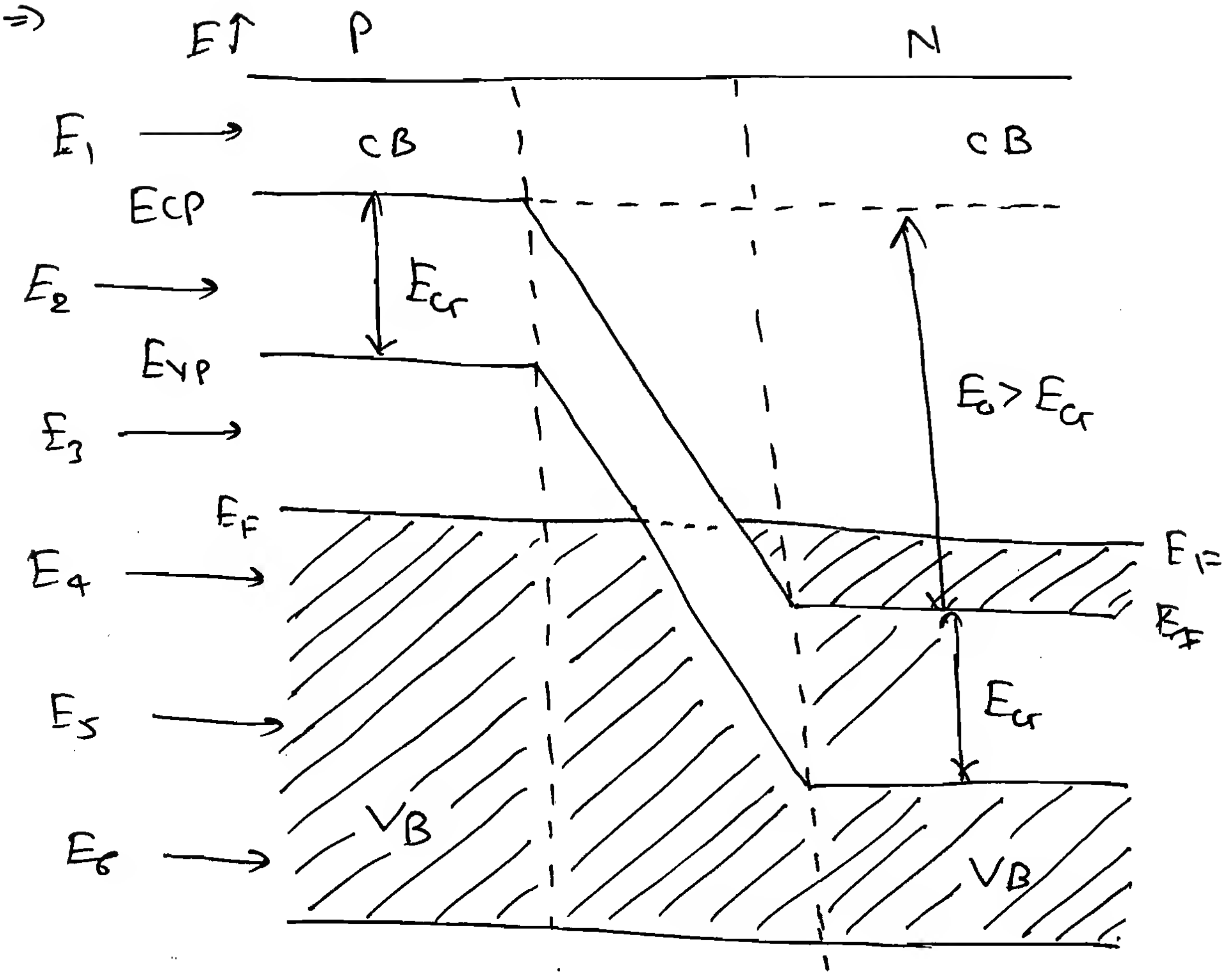
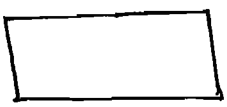
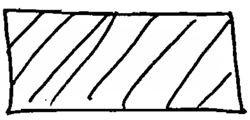
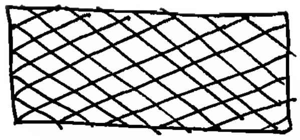
=> 

Fig - (A) : Open circuit.

=> Due to heavy doping of the order of $1:10^3$ (or) $1:10^{20}\ cm^{-3}$ width of depletion region decreases to as small as 100 Å at such narrow depletion region according to quantum mechanics a special effect called tunneling is observed based on it the diode is design. It was proposed by Esaki.

->  -> Empty State. (electron doesn't exist.)

=>  -> Filled State (electron exists).

⇒  → Filled States parallel to empty States.

→(i) Width of depletion region should be very narrow (100 Å) ✓

→ (ii) At one side of diode filled states should exists. at the other side at the same energy empty state should exists.

→ If the above two conditions are satisfy then electrons tunnels from filled to empty state.

* Open circuit:

⇒ From fig- A it can be observed that second condition of tunneling is not satisfied hence tunnelling is not possible. Hence current is zero.

⇒ V & I are zero. hence fig- A matches with point A of fig- I.

* Reverse bias:

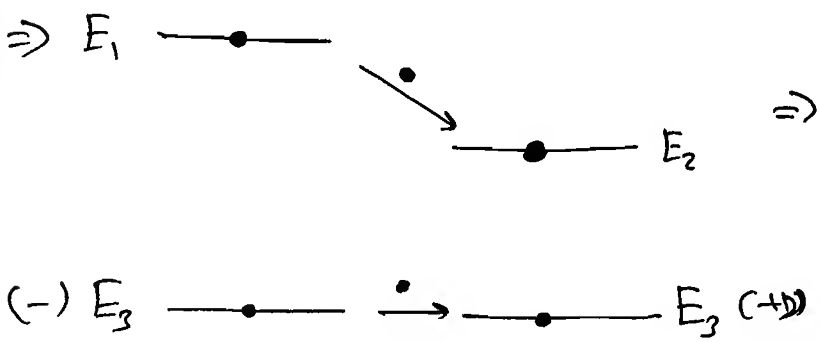
⇒ Due to Reverse bias width of depletion

region and ions of depletion region increases hence V_0 (Volts) and E_0 (eV) increase by applied reversed bias.

$E_0 = E_{cp} - E_{cn}$ is increasing implies N-side levels shift down hence fig- (A) becomes (B).

→ In fig- (B) top filled states of Valance band of p-side become parallel to bottom empty state of Conduction band of n-side. hence e^- tunnel from p to n and produce current from n-to p.

V & I are -ve hence fig- (B) matches with point -(B). as reverse bias increases n-side levels shift down more and more hence volume of tunneling and reverse current increases. i.e. excellent conduction (E.C) is possible.



⇒ Diffusion

⇒ Drift

⇒

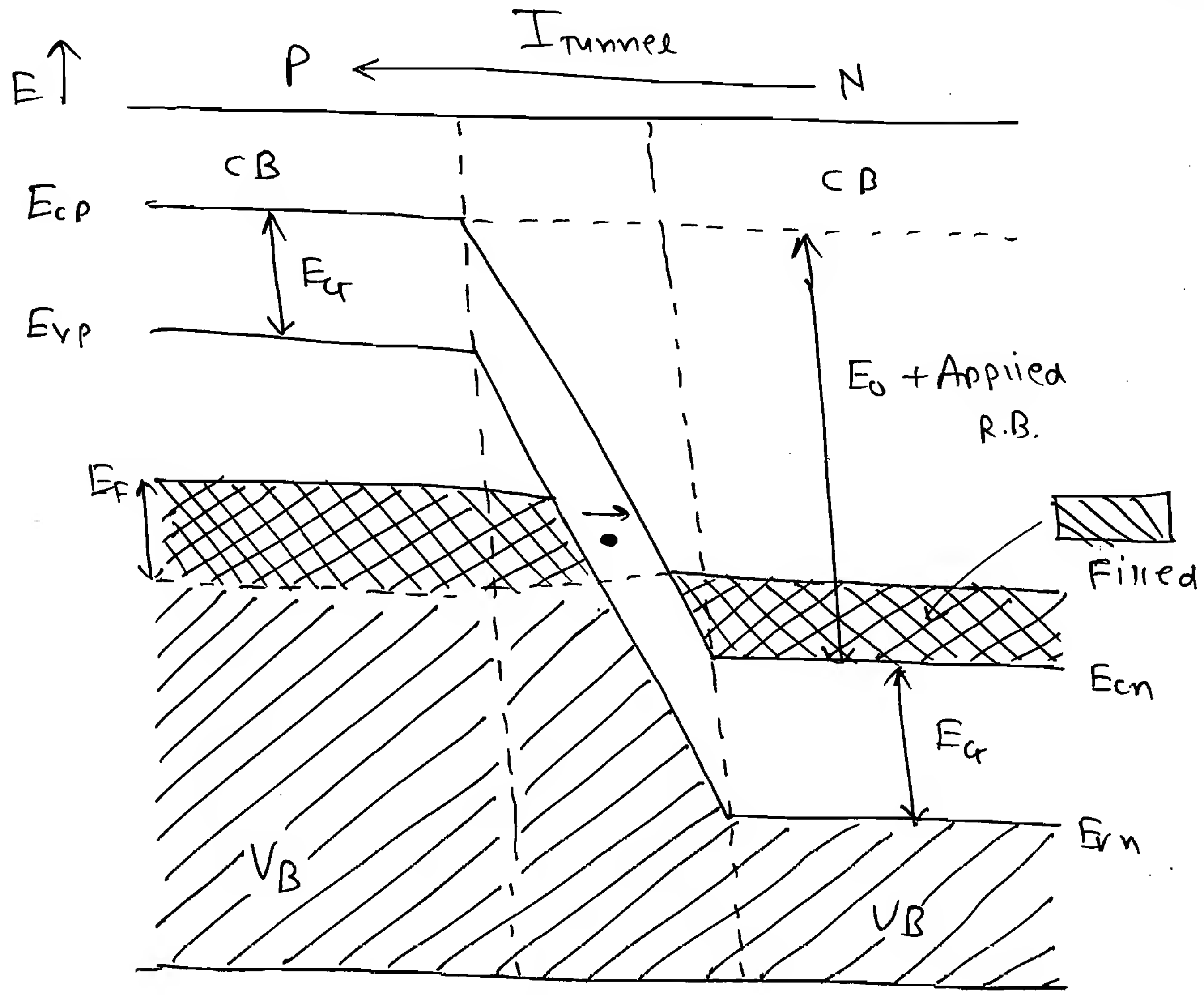


Fig- (B)

<u>Note:</u>

→ In a P-N diode $E_G > E_0$ hence energy of e^- is more than energy of hill hence to go from one side to other side of diode electron climbs down (diffussion) energy hill.

→ In a Tunnel diode $E_0 > E_G$ hence energy of e^- is less than energy of hill hence to go from one side to other side electron penetrates (Tunnels) through barrier.

⇒ Due to forward bias width of depletion region and ions of depletion region decreases hence V_0 (V) and E_0 (eV) decrease by applied forward bias.

$E_0 = E_{cp} - E_{cn}$ is decreasing implies n-sides levels move up. Hence fig - (A) becomes (C).

⇒ In fig - (C) Top filled state of conduction band of n become parallel to bottom empty states of p hence second condition of tunneling is satisfied hence electrons tunnel from N to P and produce current from P to N.

⇒ V & I are +ve hence fig - (C) matches with point (C). as forward bias increases forward current starts from 0 (point - (A)), increases (point - (C)) later on reaches a maximum (I_P), decreases (point - (D)) and finally becomes zero (point - (E)).

⇒

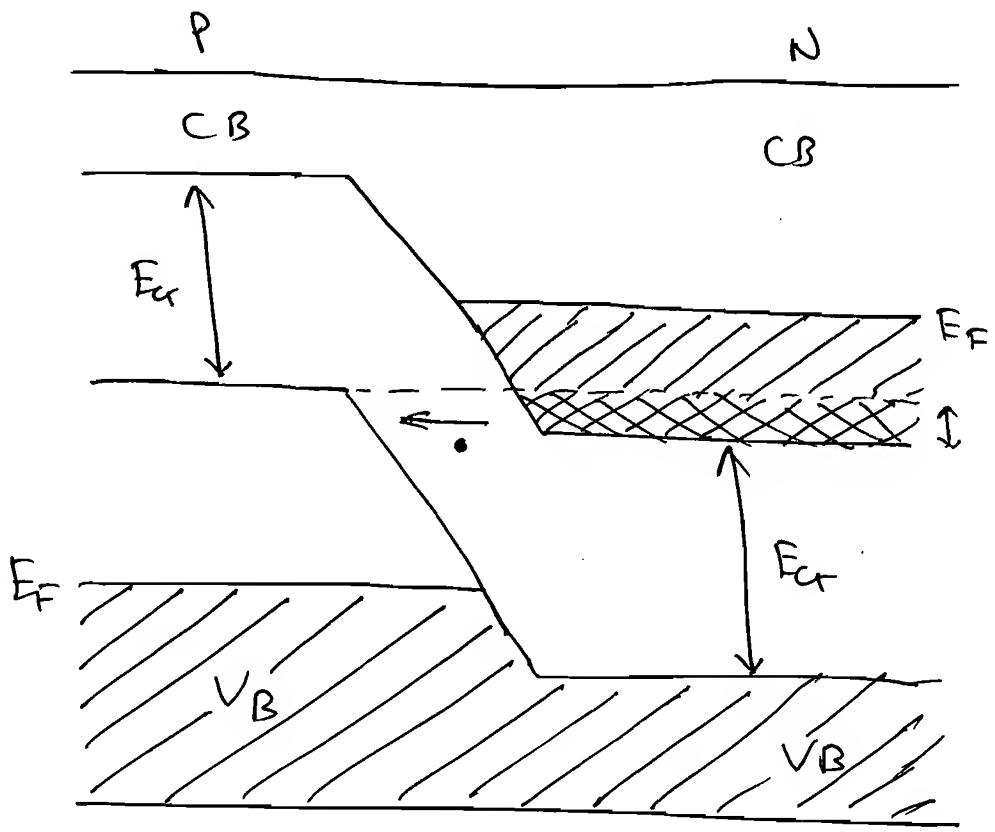


FIG-(D) FB↑↑

⇒

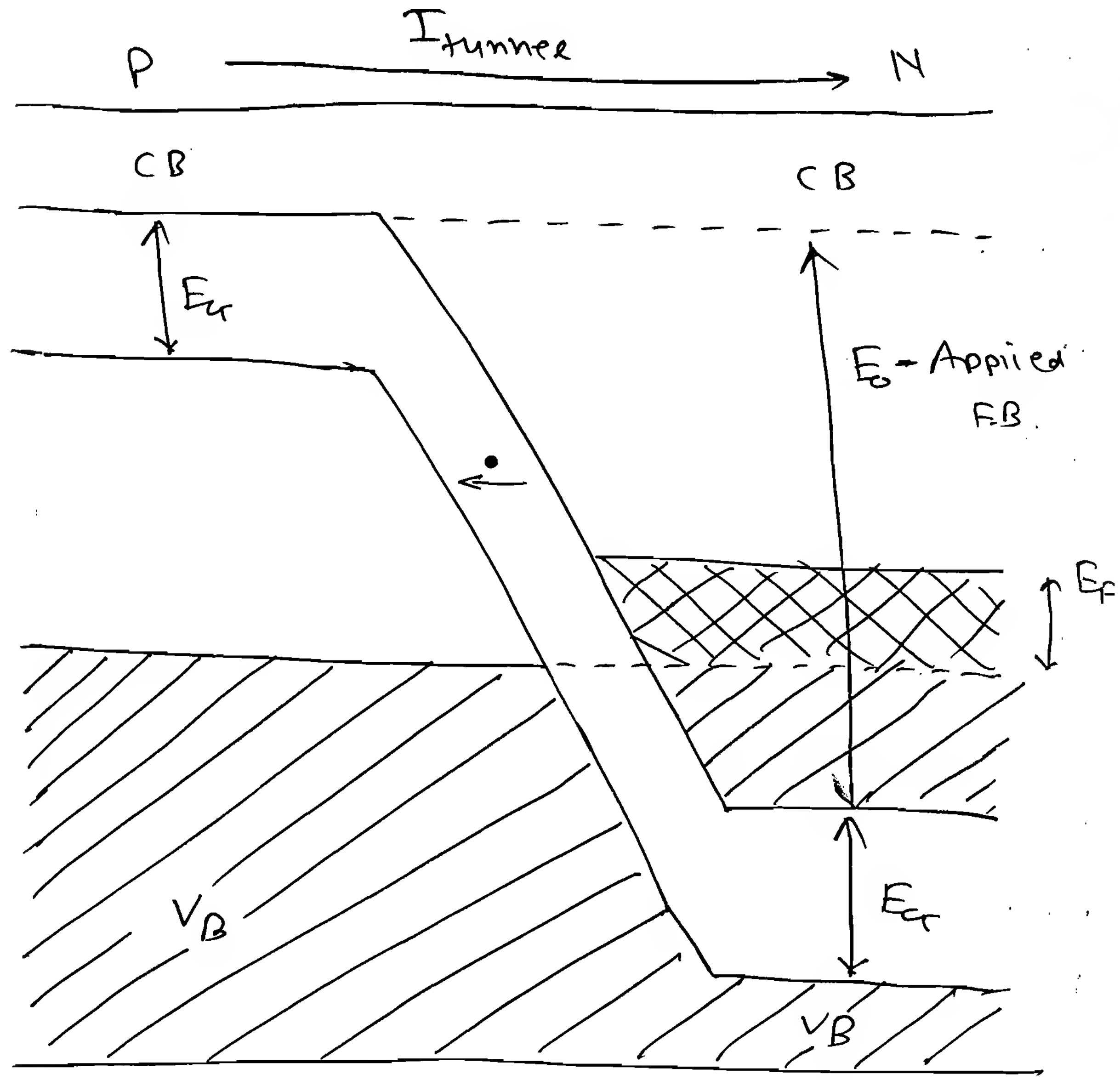


FIG-(C)

F.B.

⇒

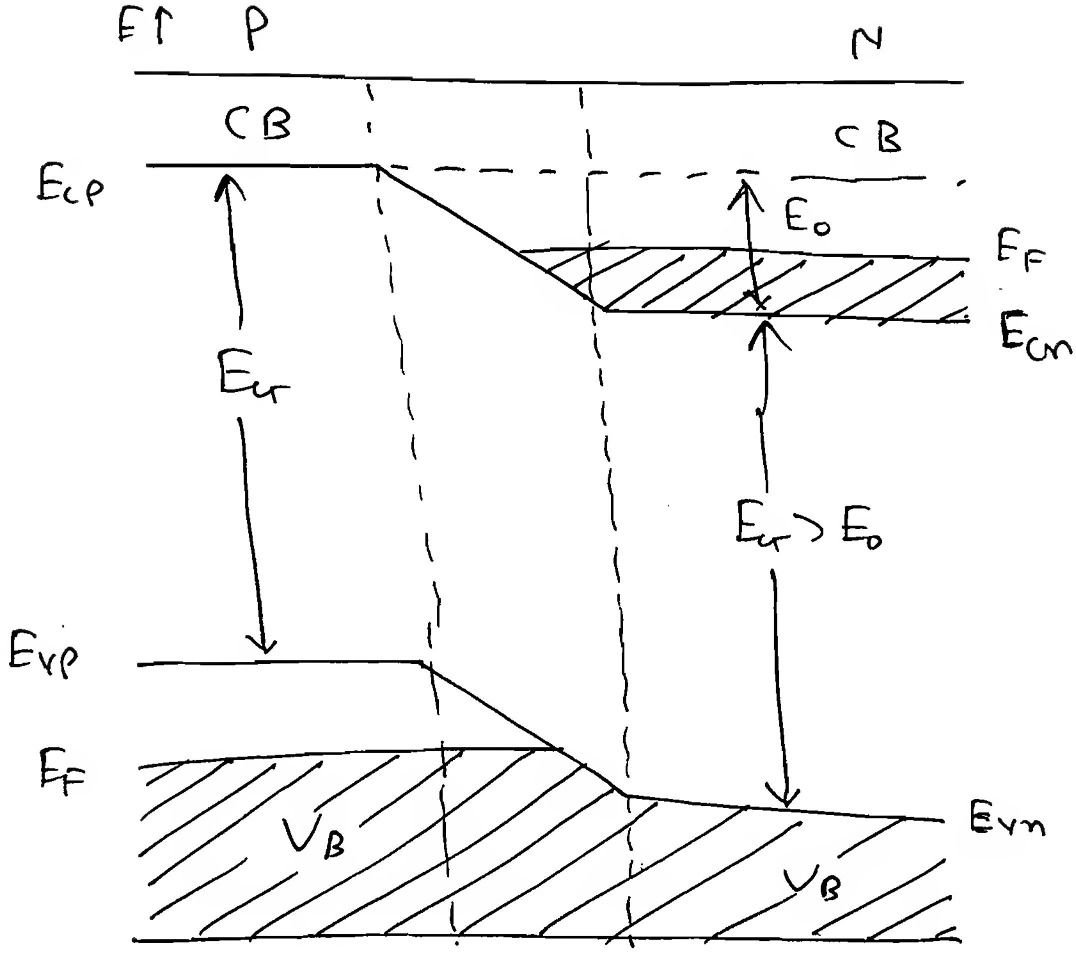
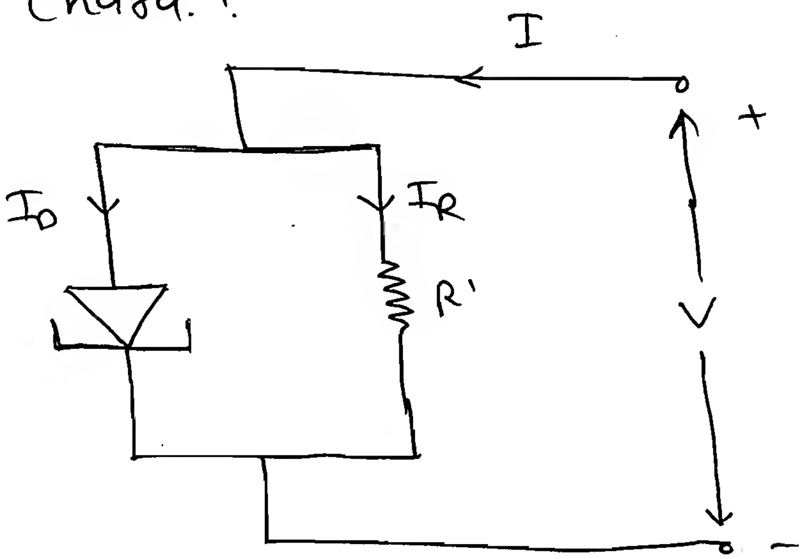


Fig - (E) - FB↑↑↑

→ Due to forward bias E_0 decreases and $E_G > E_0$ occurs (fig - (E)) which valid for a P-N diode hence from now onwards whatever current is possible in forward biased P-N diode will also be possible in forward biased tunnel diode hence forward char. of P-N diode (dash and dots) is superimpose onto forward char. of tunnel diode.

→ In FB tunnel diode I_{tunnel} flows from P→N. In FB P-N diode $I_{diffusion}$

istor R' is placed parallel to a ... rent
...nnel diode which has $\left|\frac{dI_D}{dV}\right|_{max} = 1/10\,\Omega$ ... tarting
...e value of R' such that the ... ncreases
...tion doesn't exhibit -ve region in
Chara. ?



-ve region means as voltage
increases current decreases. -ve
region should not be exibitted.
Hence $\frac{dI}{dV} \geq 0$.

$$I = I_D + I_R.$$

$$I = I_D + V/R'.$$

$$\therefore \frac{dI}{dV} = \frac{dI_D}{dV} + \frac{1}{R'}.$$

$$\frac{dI}{dV} \geq 0.$$

...e, $\frac{1}{R'} \geq \left|\frac{dI_D}{dV}\right|_{max} \longrightarrow \boxed{R' \leq 10\,\Omega}$

$\boxed{Q}$ Consider a tunnel diode under open circuit condition. Calculate width of depletion region given.

$$N_D = N_A = 4.41 \times 10^{19} \, cm^{-3}.$$

$$V_0 = 0.75 V.$$

$$\epsilon = 141.6 \times 10^{-14} \, F/cm.$$

Sol^n:

$$\omega = \sqrt{\frac{2 \epsilon V_0}{q} \left[\frac{1}{N_D} + \frac{1}{N_A} \right]}$$

$$= \sqrt{\frac{2 \times 141.6 \times 10^{-14} \times 0.75}{1.6 \times \cancel{10^{-19}}} \times \frac{2}{4.41 \times \cancel{10^{19}}}}.$$

$$\boxed{\omega = 77.7 \, A^{\circ}}$$

Note:

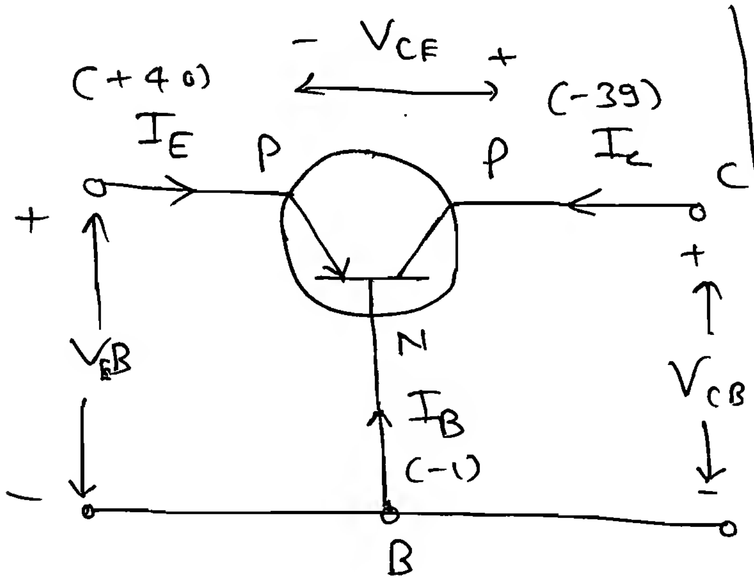
eq^n given for p-n diode for ω, x_{n0}, x_{p0}, V_0, E_0 etc can be used at any p-n j^n of any electronic device.

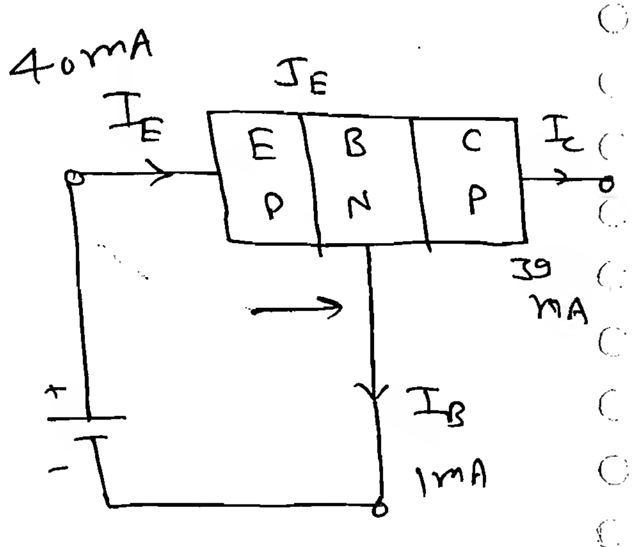
☆ Bipolar Junction Transistor :-

⇒ BJT is a 3 - terminal device found in 1947 at Bell laboratories by Bardeen, Brattain and Shockley.

⇒ In the ckt symbol, perpendicular line represents base. out of the two angular line one with arrow represents emitter. The other without arrow represents collector. The direction of arrow shows the direction of flow of current when emitter jn is FB.

⇒





⇒ **KCL**:

$$I_E + I_B + I_C = 0.$$

KVL:

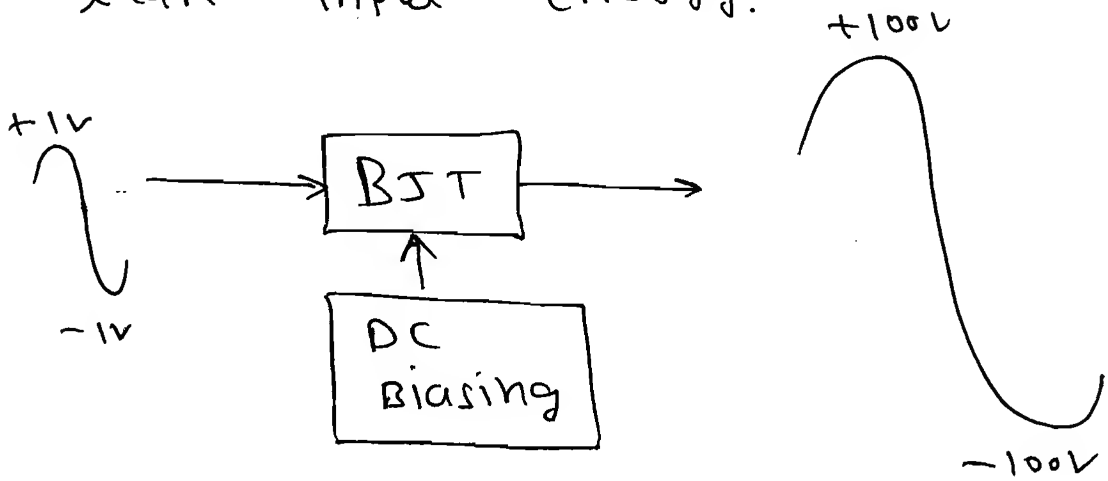
$$V_{CB} = V_{CE} + V_{EB}.$$

→ It has application like, switch, phase shifter, amplifier & oscillator.

⇒ A device is said to be giving amplification service if the following two conditions are satisfied.

① Output should be an exact replica of input.

② Output energy should be greater than input energy.



* Current Components in Common base Configuration:

(1) $I_E = I_{pE} + I_{nE} \simeq I_{pE}$.

(2) $-I_{co} = I_{CBO} = I_{pco} + I_{nco}$.

(3) $I_c = |-I_{pc1}| + I_{CBO}$.

(4) $I_c = |-\alpha I_E| + I_{CBO}$.

(5) $\alpha = -\dfrac{(I_c - I_{CBO})}{(I_E - 0)} = \dfrac{I_{pc1}}{I_E}$.

(6) $\alpha_{dc} = -(I_c | I_E)$.

(7) $\gamma^* = (I_{pE} | I_E) \simeq 1$.

(8) $\beta^* = (I_{pc1} | I_{pE}) \simeq 1$.

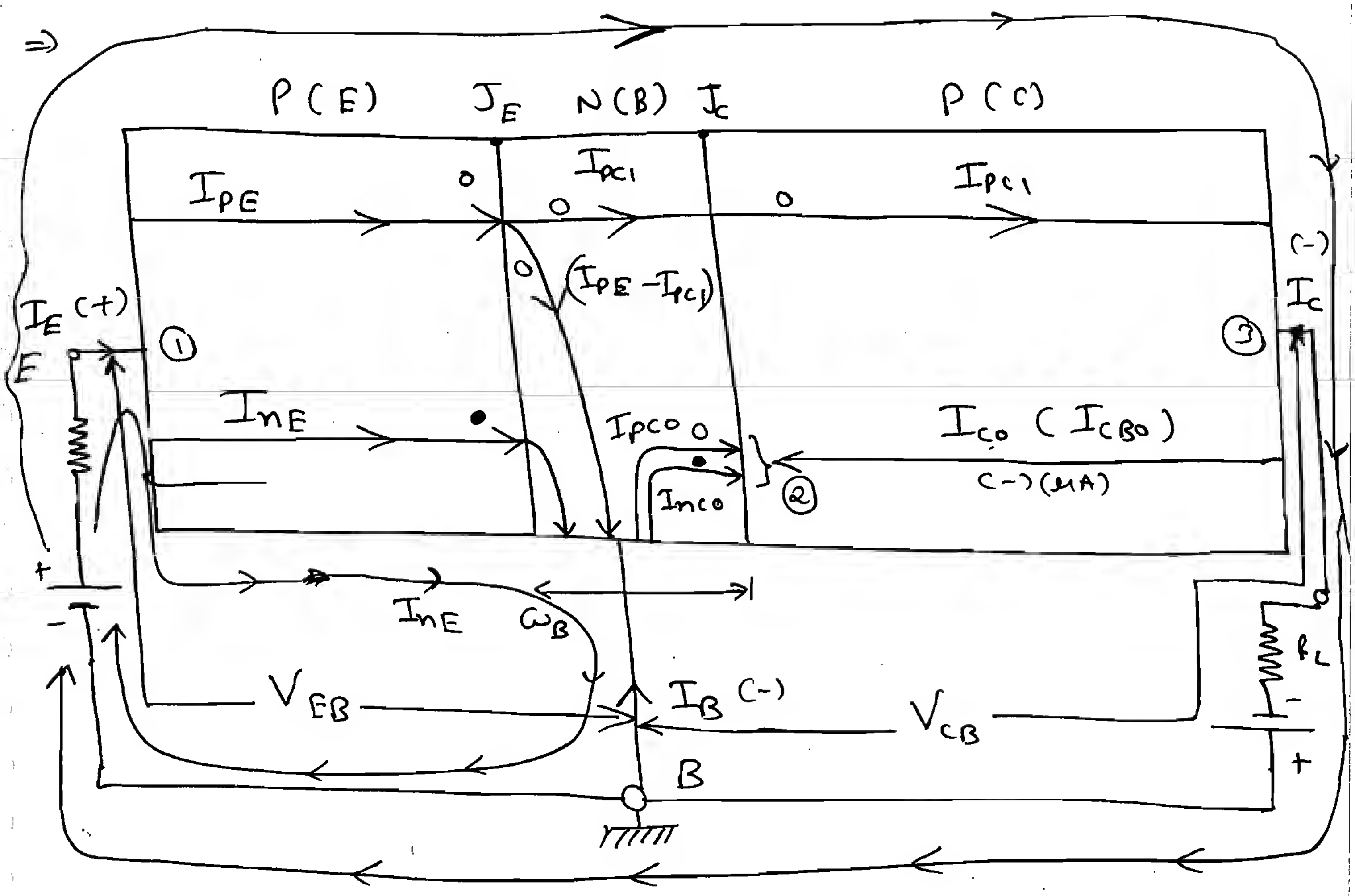
(9) $\alpha = \beta^* . \gamma^* = (I_{pc1} | I_E) \simeq 1$.

=>

	E	B	C
Doping	Heavy	Less	Modrate
Width	Modarate	Thin	Large

(1) $W_B (1\mu m) << L_p (100\mu m)$
(2) $N_D \downarrow\downarrow$
$\rightarrow I_{pc1} \simeq I_{pE}$

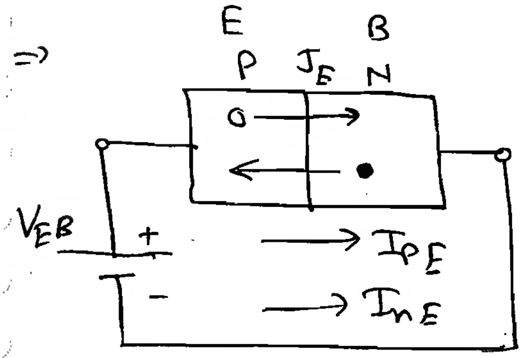
=>

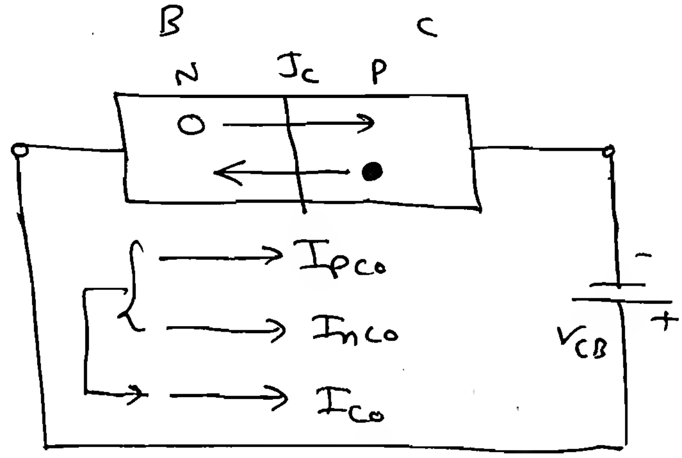


=>

J_E	J_C	R.O.O. (Region of operation)	App.
FB	FB	Saturation	ON switch
RB	RB	Cut - off	OFF switch
FB	RB	Normal Active	Amplifier
RB	FB	Inverse Active	Attenuator

=>





⇒ J_E is forward bias hence I_{pE} & I_{nE} flow from P to N.

→ I_{pE} is made up of holes out of which few holes recombine in base and go out of base ($I_{pE} - I_{pC1}$). Rest of them reach collector (I_{pC1}).

⇒ J_C is Reverse biased hence I_{pCo} & I_{nCo} flow from n to p.

→ I_{Co}, I_o at J_C flows from N to P but shown P to N hence -ve.

$$\boxed{I_{CBO} = I_{Co} + I_{SL} + I_{AM}}$$

→ I_{Co} : current due to thermally generated minority carriers.

I_{SL} : Current due to surface leakage.

I_{AM} : Current due to avalanch multiplication.

→ By applying KCL at points 1, 2 & 3 we get eqns 1, 2 & 3.

→ For the device to act as amplifier load current I_c to be large hence I_{pC1} to be large. Hence I_{pE} to be large. Hence I_E to be large

→ As input current I_E increases I_{pE}, I_{pC1} and output current I_c increases hence it is current controlled device.

→ To make I_{pC1} approximately I_{pE} recombination of holes in base to be decreased for which two conditions are proposed:

1. W_B made very much less than L_p.
   → A hole travelles L_p distance before recombination by then it crosses base and enters collector.

2. Doping of base is decrease. Hence availability of e^- in base decreases hence hole recombining probability decreases hence hole reaching collector probability increases.

→ A hole in Collector is majority Carrier hence recombination prob. is less. and it being +very Charge gets attracted by −ve supply of Collector. hence passes through load.

⇒ I_E is made of I_{PE} and I_{nE}. out of which only I_{PE} flows through load hence to make $I_{PE} \gg I_{nE}$ emitter doping heavily dopped.

⇒ Base Current I_B is made up of the following Components.

1. electron enters into base through base terminal for recombination.
2. electrons enter into base through base terminal to give I_{nE} Component.
3. electrons leave the base through base terminal to give I_{CO} Component

⇒ I_{PC1} is approximately I_{PE} and I_{PE} approximately I_E hence $I_{PC1} \simeq I_E$.
Hence I_{PC1} replaced by αI_E where

$\alpha < 1$ and Closed to 1. $\boxed{\alpha = 0.95 \text{ to } 0.995}$

Hence eqn- (3) becomes (4).

→ From- (3) & (4) we get (5) where

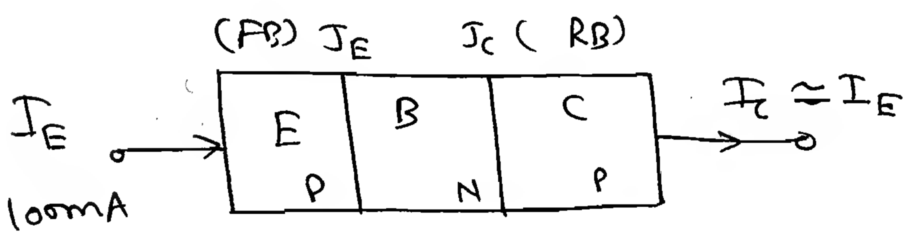
α is Common base forward current transfer ratio (or) CB current gain.

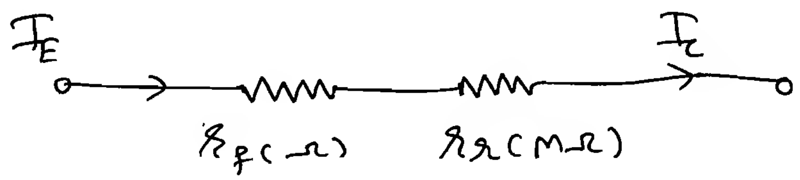
→ In eqn- (5) neglecting I_{EBO} we get (6).

⇒ γ^* : emitter efficiency (or) emitter injection efficiency.

β^* : Transport factor (or) base Transport factor.

⇒





⇒ $P_C \, (I_C^2 r_r) > P_E \, (I_E^2 . r_f)$

$P_C \downarrow = (I_C \downarrow)^2 . r_r$

$\underline{P_C} \uparrow \rightarrow \underline{T_{jC}} \uparrow \rightarrow I_{CBO} \uparrow \rightarrow I_C \uparrow \rightarrow$

Thermal Run away

$\left(\dfrac{P_C}{(\text{Area}) \uparrow} \right) \downarrow$

⇒ over at collector junction P_c is large. hence Collector j^n T_{jc} increases. hence I_{CBO} increases. hence I_c increases. hence P_c increases. which an itterative process due to which at some time excessive power (or) Temp. occurs at Collector j^n and transisters burns away called thermal run-away.

⇒ To safe guard the Transistor, Collector made large in size & hence power per unit area ~~decreases~~ at J_c decreases.

⇒ Base thin implies thinner than L_p followed by thinner than emitter and Collector

⇒ $$A_V = \frac{V_o}{V_i} = \cancel{r_f} \cdot \frac{\cancel{I_c} \cdot r_r}{\cancel{I_E} \cdot r_f} > 1 \qquad (\because r_r = M\Omega,\ r_f = \Omega).$$

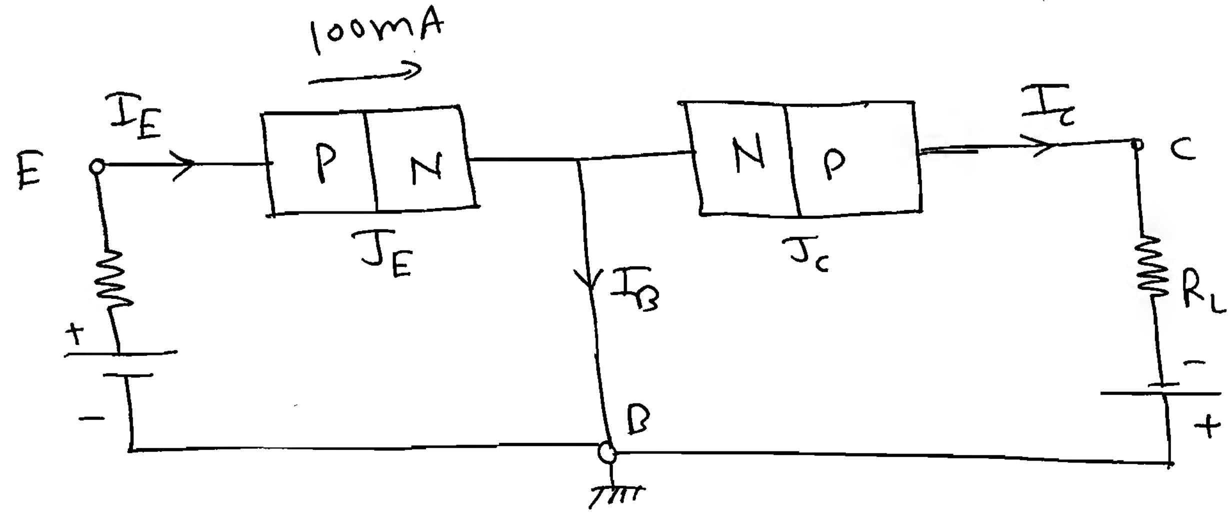
$$\therefore A_I = \frac{I_c}{I_E} < 1.$$

	A_V	A_I
CB →	✓	×
CE →	✓	✓
CC →	×	✓

* Two P-N Diode connected back to back Series can not act as Transistor (Amplifier):

Imp Concept

⇒



⇒ By making base thin in size and less dopped recombination of holes in base is not allowed hence large current I_E is forcebuly transfer from Low resistance (J_E, FB) to high resistance (J_c, RB) . Hence, Tru **Transfer Resistor Property** is ~~exhibited~~ exhibited.

⇒ Two Polarities of charge carriers are crossing junctions to give current in device which is exhibiting transfer

resistor property.

→ Hence called <u>Bipolar Junction Transistor</u>
(BJT).

⇒ Transfer Resistor

Bipolar Junction Transistor (BJT).

Two Polarities

* Early Effect (or) Base width Modulation:

(or) Base narrowing:

⇒ W_B : Physical (or) Metarilgical Base width.

W_B' : effective (or) undepleted Base width.

W_d : Width of depletion region.

⇒ J_E is FB hence width of depletion region & ions of depletion region decreases. hence V_0 decreases by V_{EB}. The applied forward bias J_C is reversed bias hence width of depletion region and ions of depletion region increases hence V_0 increases by V_{CB},

the applied reverse biased.

⇒

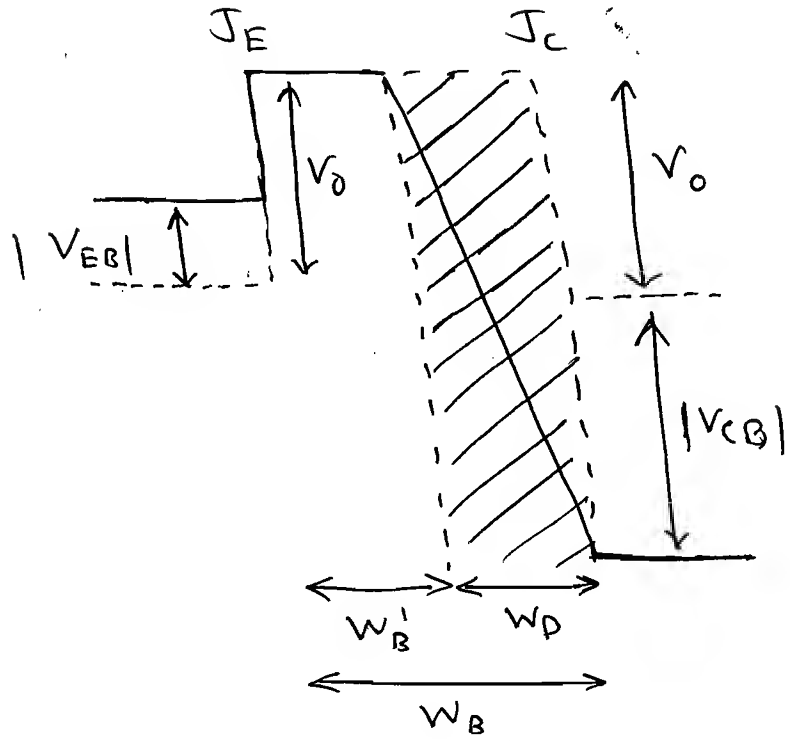


Fig- ①

⇒

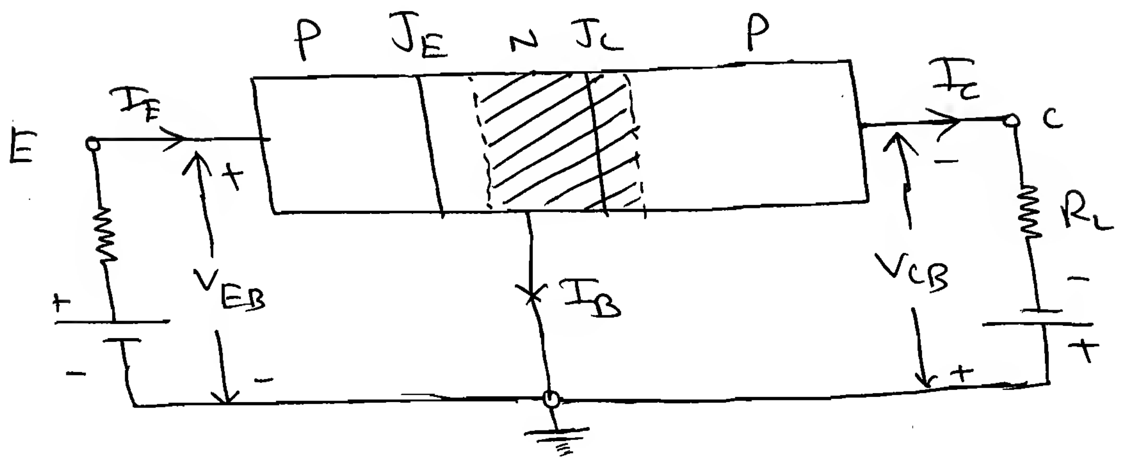


Fig- ②

⇒

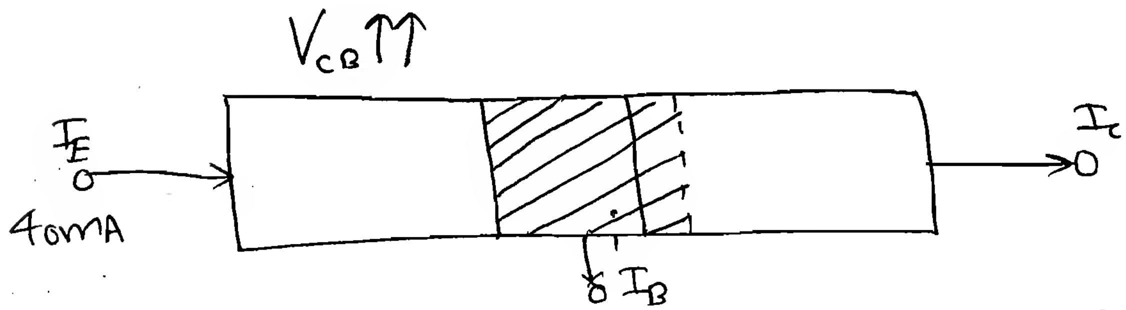


Fig-③

⇒ **Early effect No. 1:**

⇒ As reverse bias to J_c increases width of depletion region at J_c and penetration of depletion region into base increases. Hence undepleted width W_B' decreases hence charge carriers which where sitting in a width of W_B earlier will now get confined to a smaller width of W_B' hence concentration gradiant increases. J_E is forward bias hence majority carrier diffusion supports currents where diffusion is proportional to concentration gradient which is increasing hence I_E increases.

$$\Rightarrow \quad I = \left[-q D_p \left(\frac{dP}{(dx)\downarrow}\right)\uparrow\right]\uparrow$$

⇒ **Early effect No. 2:**

⇒ As reverse Bias J_c increases more & more width of depletion region & penetration of depletion region increases more and more. Hence W_B' decreases more and more. earier with a width

of $W_B < L_p$ available for recombination, recombination was less. Now with a width of W_B' very much less than L_p available for recombination, recombination further decreases. Hence, I_B decreases, I_C increases and hence α increases.

⇒ **Early effect No. - 3:**

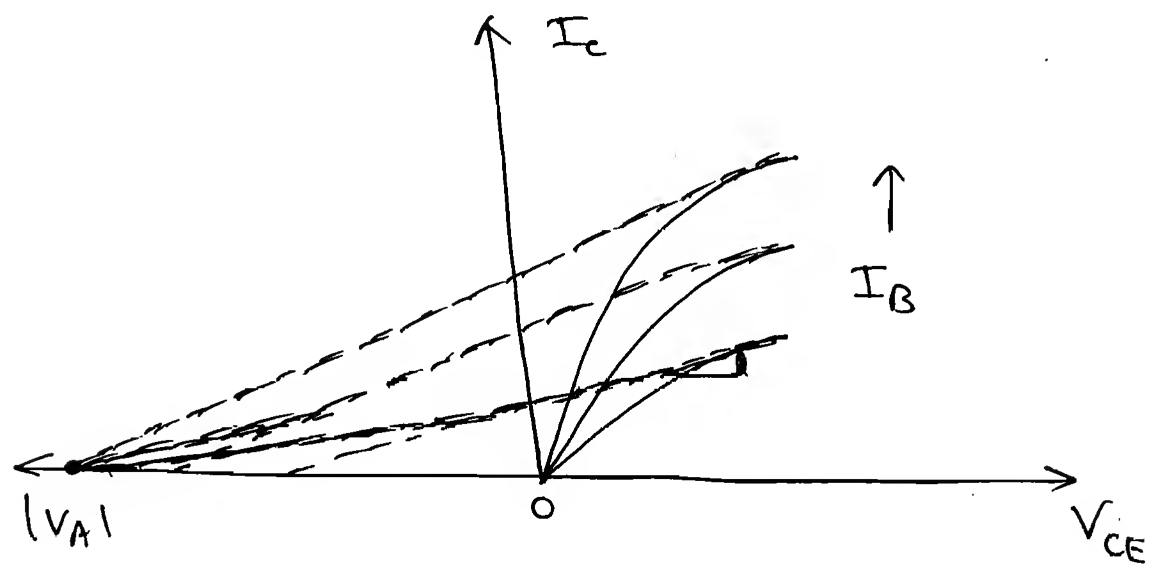
⇒ At large reverse bias to J_C width of depletion region increases and completely fills the base hence undepleted width W_B' and I_B become zero hence transistor can not act as amplifier i.e. Usefullness of Transistor as amplifier is terminated. Earlier depletion region was confined to J_C Now it is has reached J_E hence called punch through (or) reach through.

⇒ The above three effects where observed by J.M. Early. Hence called early effect.

→ out of W_B only W_B' is usefull for recombination hence called effective base width.

→ Change in V_{CB} changes $W_{B'}$ hence called base width modulation. as V_{CB} increases W_B' decreases hence called base narrowing.

⇒



⇒

$$\boxed{\begin{aligned} r_o &= \frac{|V_A|}{I_c} \\ I_c &= \alpha I_o \cdot e^{V_{BE}/nV_T}\left(1 + \frac{V_{CE}}{V_A}\right). \end{aligned}}$$

r_o: Output resistance.

V_A: Early Voltage.

* Avalanch Breakdown:

⇒ As reverse biased to J_c increases more and more, at a perticular Voltage J_c undergoes avalanch BD hence avalanch multipiication starts hence Charge Carriers and I_c increases uncontorollably hence again usefullness gets terminated. this time due to avalanch BD and earier due to punch through.

⇒ $\boxed{CB}$:

$$M = \frac{1}{\left[1 - \left(\frac{V_{CB}}{BV_{CBO}}\right)^n\right]} \qquad \boxed{n = 2 \text{ to } 10}$$

$\boxed{CE}$: $BV_{CEO} = BV_{CBO}\left(\frac{1}{\beta}\right)^{1/n}$.

$$\text{Max-Rating} = \text{MIN}\,(BV_{PT},\ BV_{AB}).$$

⇒ M : Multipiication factor due to avalanch Multipiication.

BV_{CBO} : Break down Voltage in CB with

emitter open. is defined as reverse bias at J_c in CB at which avalanch BD occurs.

→ **BV_{CEO}** : Break Down Voltage in CE with Base open is defined as RB at J_c in CE at which avalanch BD occurs.

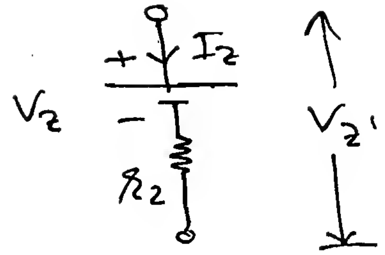
→ **BV_{PT}** : Break Down Voltage at which punch through occurs. It is independent of configuration.

→ **BV_{AB}** : Break Down Voltage at which avalanch Break Down occurs.

→ **Max_Rating** :- maximum rating is defined as maximum reverse bias that can be safely applied across J_c.

Q A zener diode has a eqn resistance of 20 Ω in BD given Voltage across zener diode is 5.2V at $I_z = 1mA$. Determine Voltage across diode at $I_z = 10mA$.

Sol^n:



$$V_z' = V_z + I_z \cdot r_z.$$

$$5.2 = V_z + (1\,mA)(20)$$

$$V_z = 5.18\,V.$$

at $I_z = 10\,mA$

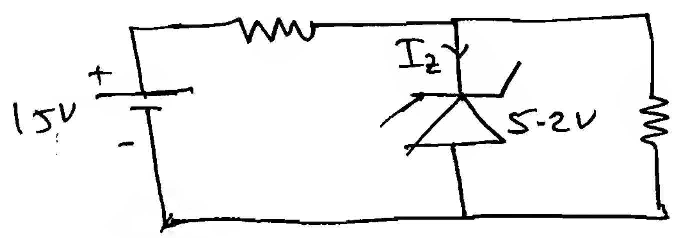
$$\therefore V_z' = 5.18 + (10\,mA)(20)$$

$$\therefore \boxed{V_z' = 5.38\,V}$$

Note:

⇒ If current through zener diode changes voltage across zener diode changes due to change in drop across r_z. But V_z and r_z or are constant.

The maximum rating of zener diode shown in ckt is 260 mW it maintains a constant voltage if current through zener diode doesn't fall below 90% of max. permisible current find the range of I_z for zener diode to act as regulator safely.



Sol^n: $260\,mW = P_{z(max)} = \overset{5.2V}{V_z} \times I_{z(max)}$

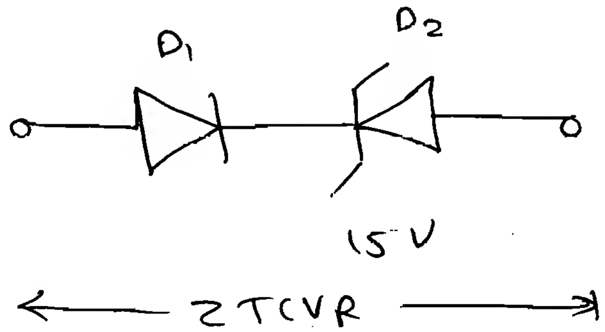
$$\boxed{I_{z(max)} = 50\,mA}$$

90% of $I_{z(max)} = 45\,mA = I_{z(min)}$.

$\downarrow$

50 mA

Q In the given ckt temp. coefficient of D_1 is $-1.7\,mV/^\circ C$. The series combination is used to construct a zero temp. coefficient voltage reference. (ZTCVR) find in $\%/^\circ C$ the required temp. coefficient of D_2.



Soln:

Note: A ZTCVR should maintain constant voltage irrespective of fluctuation in temperature.

$D_2: \quad +1.7 \times 10^{-3} \frac{V}{^\circ C} \times \frac{100}{15} = +0.01133\ \%/^\circ C.$

Q For a BJT $\beta = 100$ collector junction BD voltage in common base width Emitter open $= 120\,V$. Assuming empirical constant as 3, calculate collector j^n

BD Voltage in CE in with base open.

Soln:

$$BV_{CEO} = \underset{\downarrow\,120V}{BV_{CBO}} \left(\frac{1}{\underset{\downarrow\,100}{\beta}}\right)^{1/n}.$$

$$BV_{CEO} = 120 \times \left(\frac{1}{100}\right)^{1/3}.$$

$$\boxed{BV_{CEO} = 25.85\ V}$$

Imp:

Q for BJT $I_c = 1mA$ at $V_{CE} = 1V$. given early voltage as 75 V. Calculate I_c at $V_{CE} = 10V$. assume α as constant.

Soln:

$$I_c = \underbrace{\alpha I_o . e^{V_{BE}/nV_T}}_{x} \left(1 + \frac{V_{CE}}{V_A}\right).$$

$$\therefore \frac{I_c'}{1mA} = \frac{\cancel{x}\left(1 + \frac{10}{75}\right)}{\cancel{x}\left(1 + \frac{1}{75}\right)}.$$

$$\therefore I_c' = \frac{85}{76}\ mA.$$

$$\therefore \boxed{I_c' = 1.118 mA.}$$

Q Find O/P R of BJT given early voltage as 150V and collector current 0.1 mA.

Soln:

$$r_o = \frac{|V_A|}{I_c} = 1.5 M\Omega$$

Q A Ge PNP transistor is biased in active region given diffussion current at Emitter jn as 0.298mA. Calculate dynamic emitter Resistance.

Soln:

$$r_E = \frac{\eta V_T}{I_E}$$

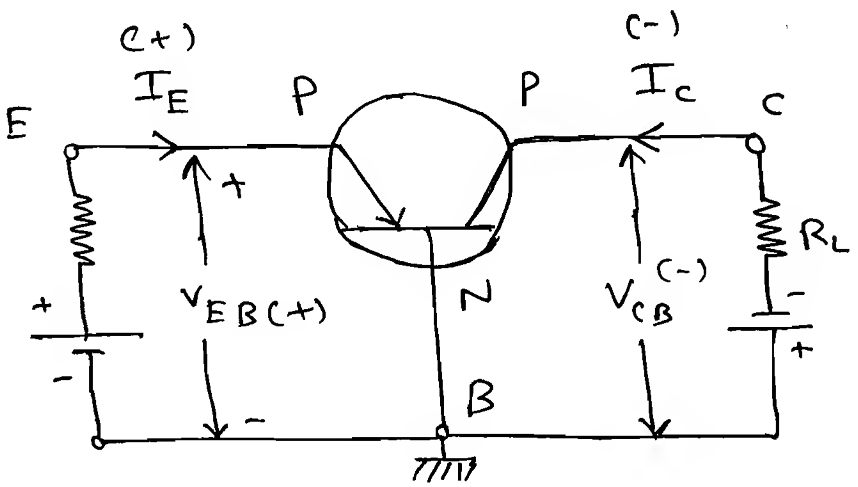
$$= \frac{1 \times 0.026}{0.298 \times 10^{-3}}$$

$$\therefore r_E = 87.24 \ \Omega.$$

$$\therefore \boxed{r_E = 87.24 \ \Omega}$$

* Input and output characteristic of CB (or) Grounded base configuration:

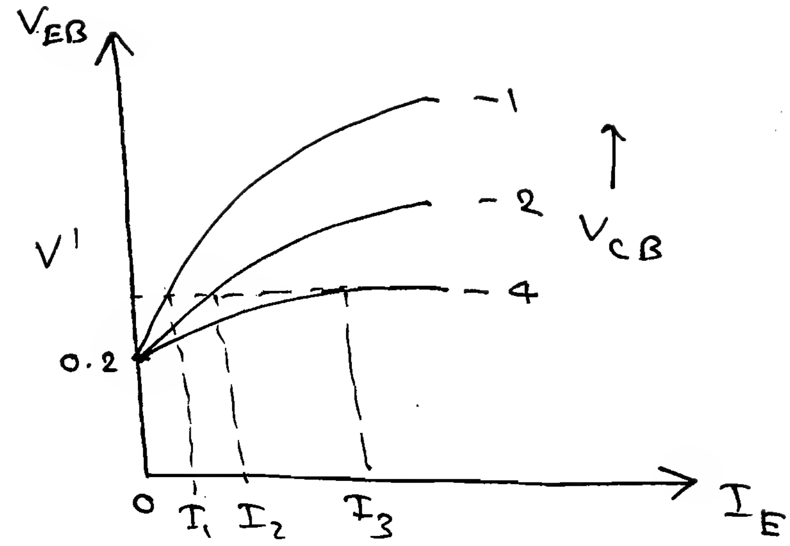
⇒



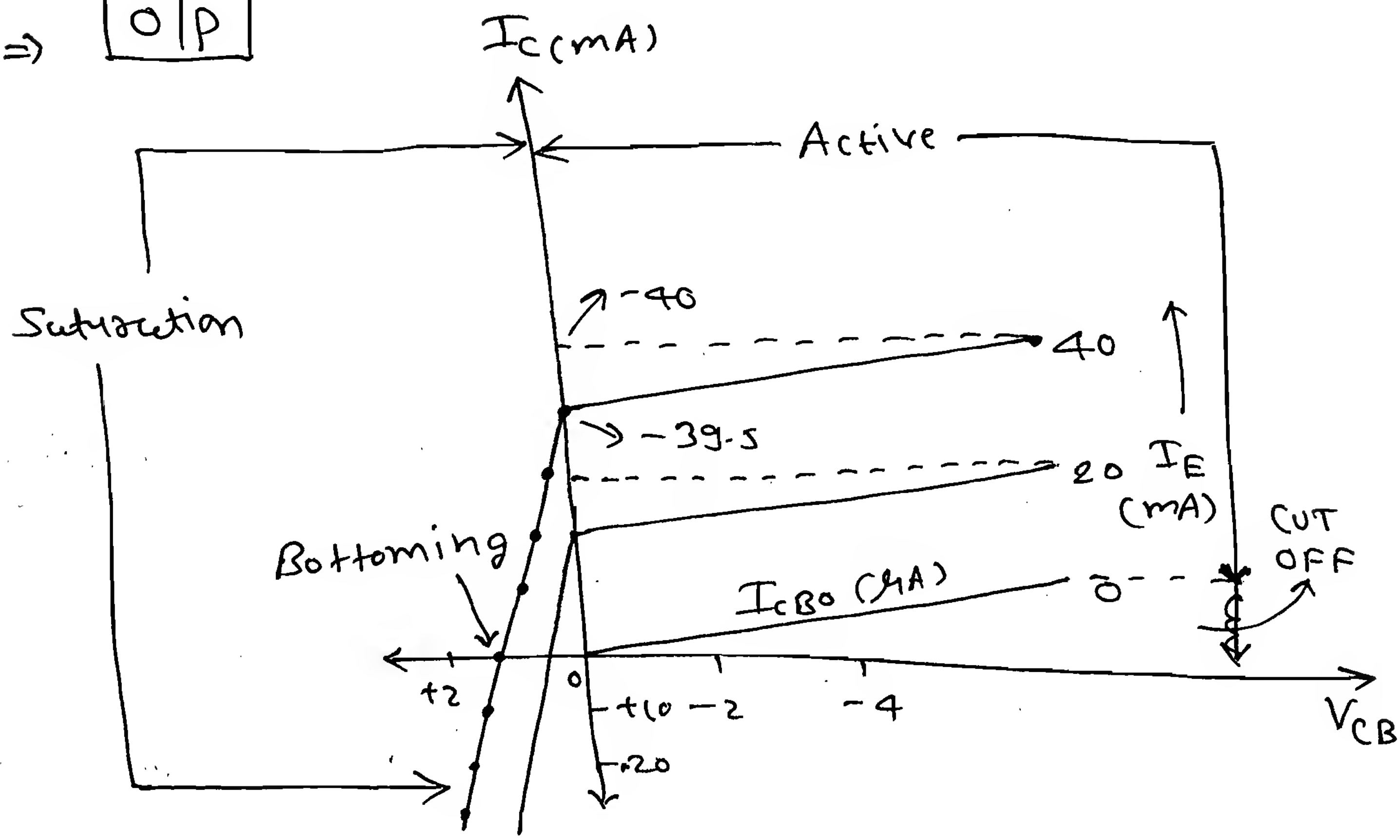
I.V. ⟶ I_E, V_{CB}

D.V. ⟶ V_{EB}, I_c.

⇒ I/P



⇒ O/P



⇒ I.V. : Independent Variable.

D.V. : Dependent Variable.

* <u>Input characterestics:</u>

⇒ I/P chara. of CB configuration concept wise looks similar to forward char. of P-N diode since V_{EB} and I_E are

are Voltage across and current through forward biased emitter in diode. the Shape doesn't match since x-axis and y-axis are interchanged.

⇒ As Reversed bias to J_c increases according to early effect ① I_E increases hence input current shift down.

* <u>output Characteristics:</u>

⇒ <u>Active Region:</u>

→ $I_c = -\alpha I_E + I_{CBO}$.

→ Say $I_E = 0$, then $I_c = I_{CBO}$ is Constant. irrespective of V_{CB}.

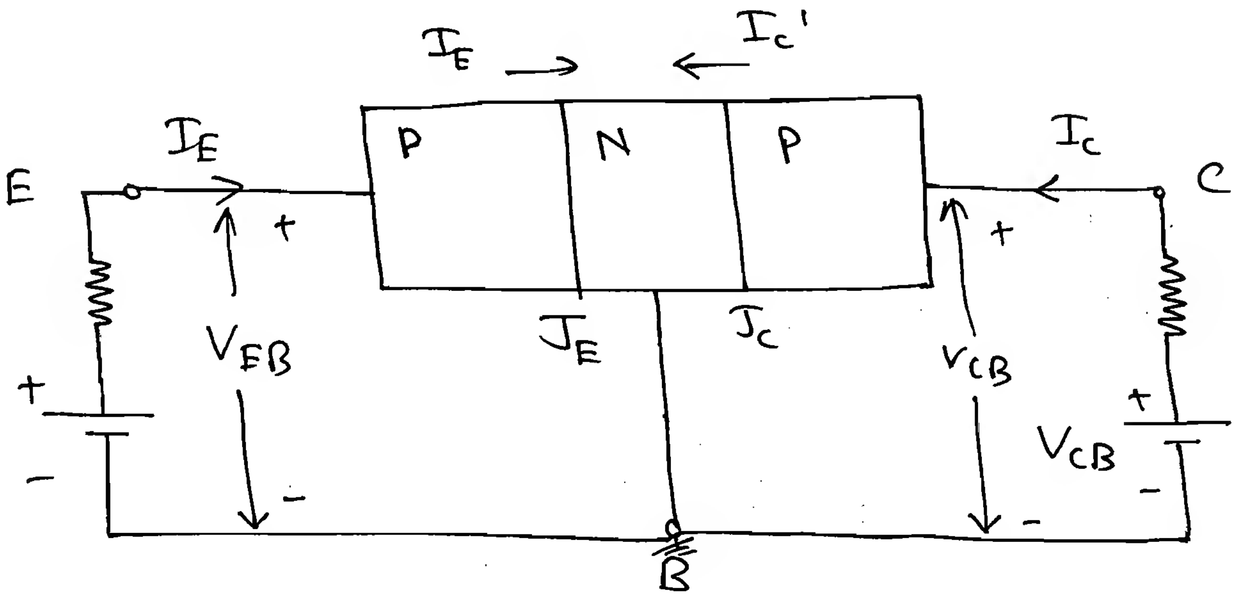
→ Say $I_E = 40mA$, then I_{CBO} gets neglacted. as reversed biased to J_c increases according to early effect ② α increases. $\alpha < 1$ and closed to 1. If it increases, finally it becomes one hence I_c starts from less than I_E and closed to I_E, increases and finally becomes I_E. Hence Curves are almost Straight line i.e. not much slope is existing.

$$\Rightarrow \quad I_C = -\alpha I_E + \cancel{I_{CBO}}$$

$\alpha < 1$ $\xrightarrow[\text{EE ② } \rightarrow \ \alpha \uparrow]{\text{As RB To } J_C \uparrow}$ $\alpha = 1$

$|I_C| < |I_E|$ $\qquad\qquad$ $|I_C| = |I_E|$.

⇒ Saturation:



$$\Rightarrow \boxed{V_{EB} = \text{Constant}}$$

V_{CB}	I_E	I_C'	Net Current	I_C (mA)
+0.5	40	10	$\overrightarrow{30}$	−30
+1.5	40	40	0	0
+2.0	40	50	$\overleftarrow{10}$	+10.

⇒ As V_{CB} Forward biased to J_C increases I_C changes from −ve to zero to +ve

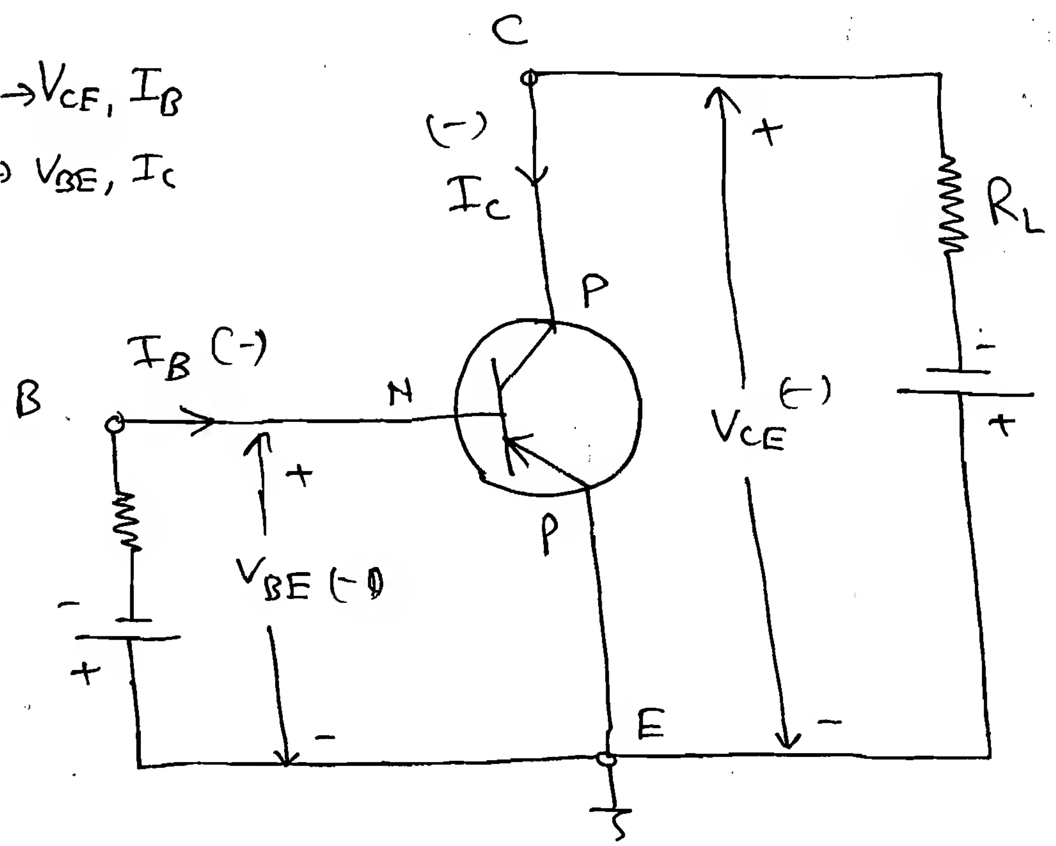
⇒ For different values of I_E, all the curves are touching the bottom at x-axis hence bottoming is said to have occurred.

* Input and output Characteristic of CE (OR) Grounded Emitter Configuration:

⇒

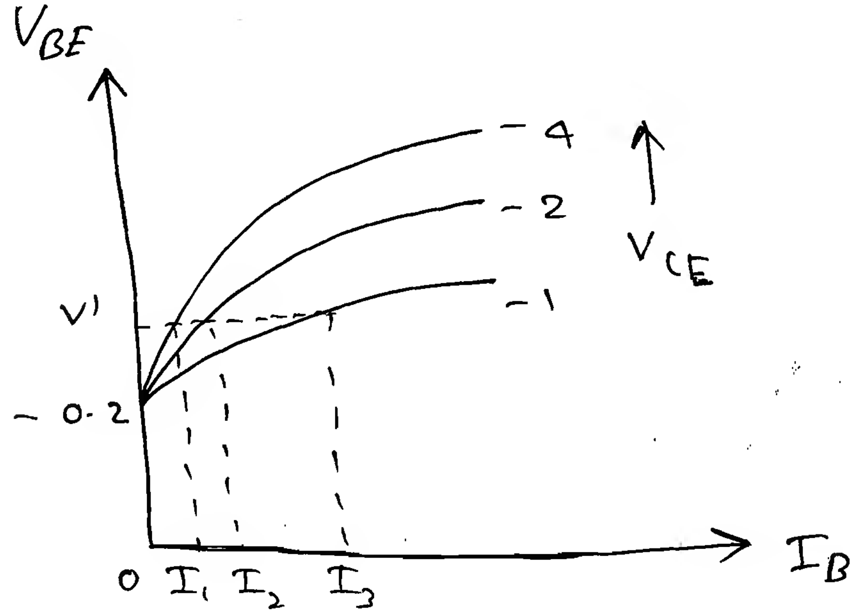
I.V. :→ V_{CE}, I_B

D.V. :→ V_{BE}, I_C

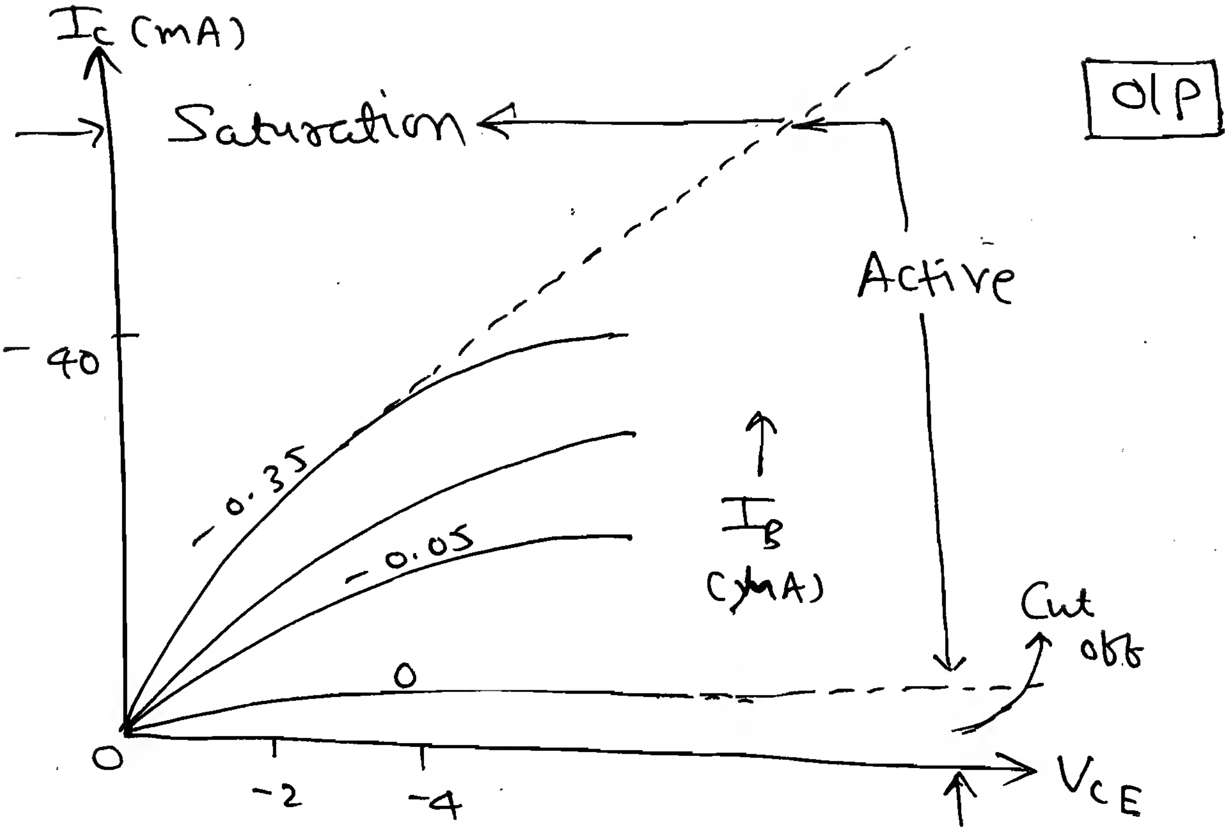


⇒

I/P



⇒



⇒

$$I_C = (1+\beta) I_{CBO} + \beta I_B .$$

$$\beta = \frac{I_C - I_{CBO}}{I_B + I_{CBO}} = \frac{\alpha}{1-\alpha} .$$

$$\beta_{dc} = \frac{I_C}{I_B} = \frac{\alpha_{dc}}{1-\alpha_{dc}} .$$

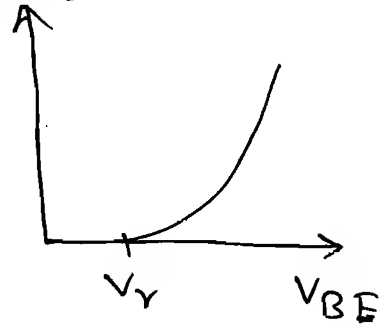
* Input Characterestics:

⇒ Input char. of CE configuration concept wise look similar to forward char. of P-N diode since V_{BE} and I_B (proportional to $\propto I_E$) are voltage across and current through forward biased emitter j^n diode.

the shape doesn't match since x-axis & y + axis are interchanged.

⇒ As reversed biased to J_c increases early effect - ② says α increases hence I_c increases hence I_B decreases. i.e. input curves move up.

⇒ $I_B \; \alpha \; I_E$



$$I_E = I_B + I_c$$

$$(mA): \; 1\,mA\uparrow = 0.01\,mA\uparrow + 0.99\,mA\uparrow$$

As RB To $J_c \uparrow \longrightarrow$ EE ② $\rightarrow \alpha\uparrow \rightarrow \alpha\uparrow = \dfrac{I_c\uparrow}{\boxed{I_E}}$

$$\rightarrow \boxed{I_E} = I_B\downarrow + I_c\uparrow.$$

⇒ CE Saturation Resistance (R_{CEsat}):

$$\boxed{R_{CE(sat)} = \frac{V_{CE(sat)}}{I_c}}$$

→ I_{CBO} : Collector current with collector j^n RB. in CB with emitter open.

→ I_{CEO} : Collector current with collector j^n RB in CE with base open.

→ β : Common emitter forward current Transfer ratio. (OR) CE current gain.

* Proof of Current gain:

① **Mathamaticaly:**

⇒ α is a number < 1 and closed to 1.

Hence $\beta = \left(\frac{I_C}{I_B}\right) > 1$ i.e. output current I_C greater than input current I_B.

② **Logicaly:**

⇒ For a small change in input current I_B there is a large change in output current I_C hence current gain exists.

$$I_E = I_B + I_C$$

$$(mA): 1mA = 0.01mA\uparrow + 0.99mA\uparrow$$

③ **Graphicaly:**

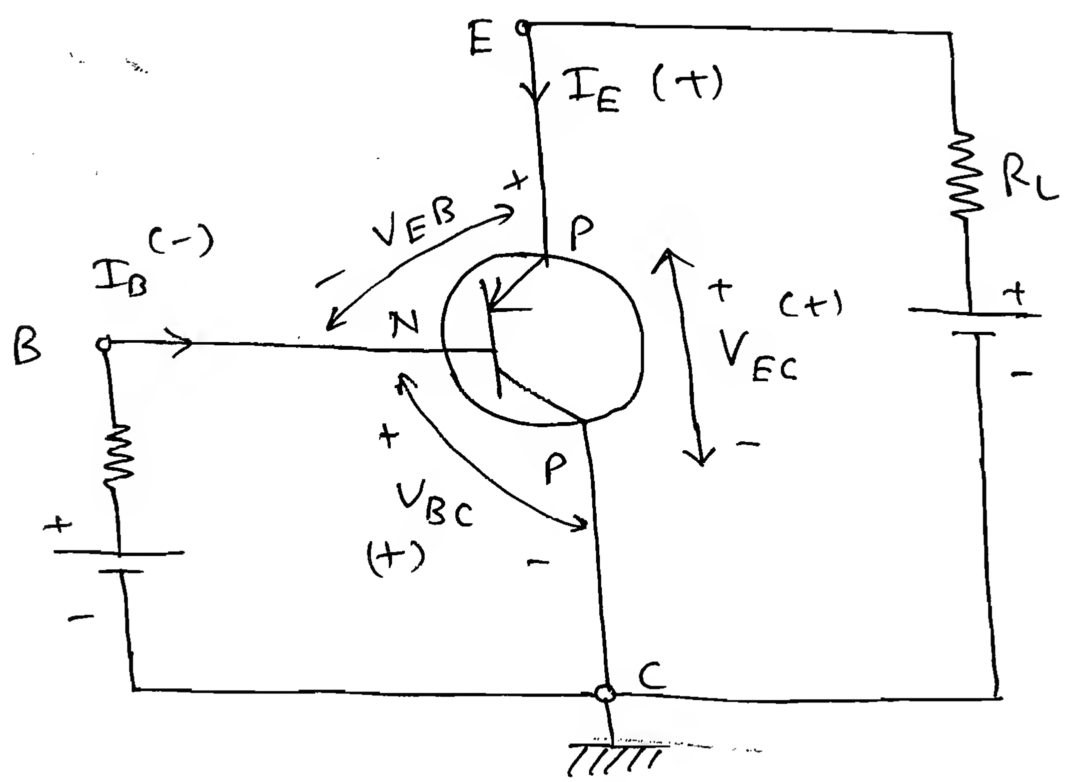
⇒ In o/p Char. a slope is existing hence current gain possible.

④ Practically:

⇒ In CE amplifier experiment existance of current gain can be observed.

* Input and Output charactere stics in CC (or) grounded Collector Config

⇒



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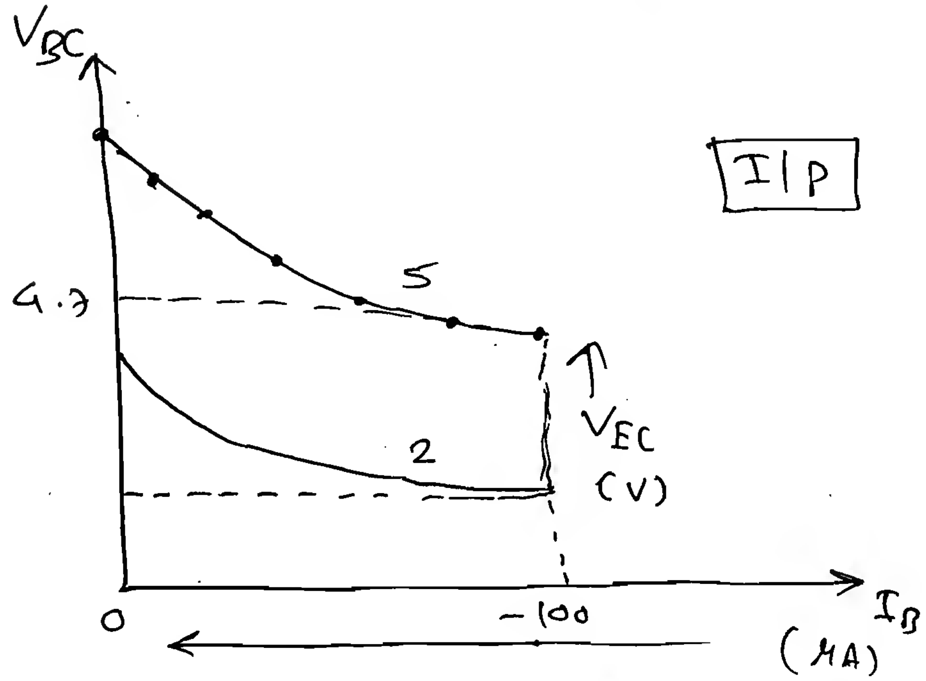

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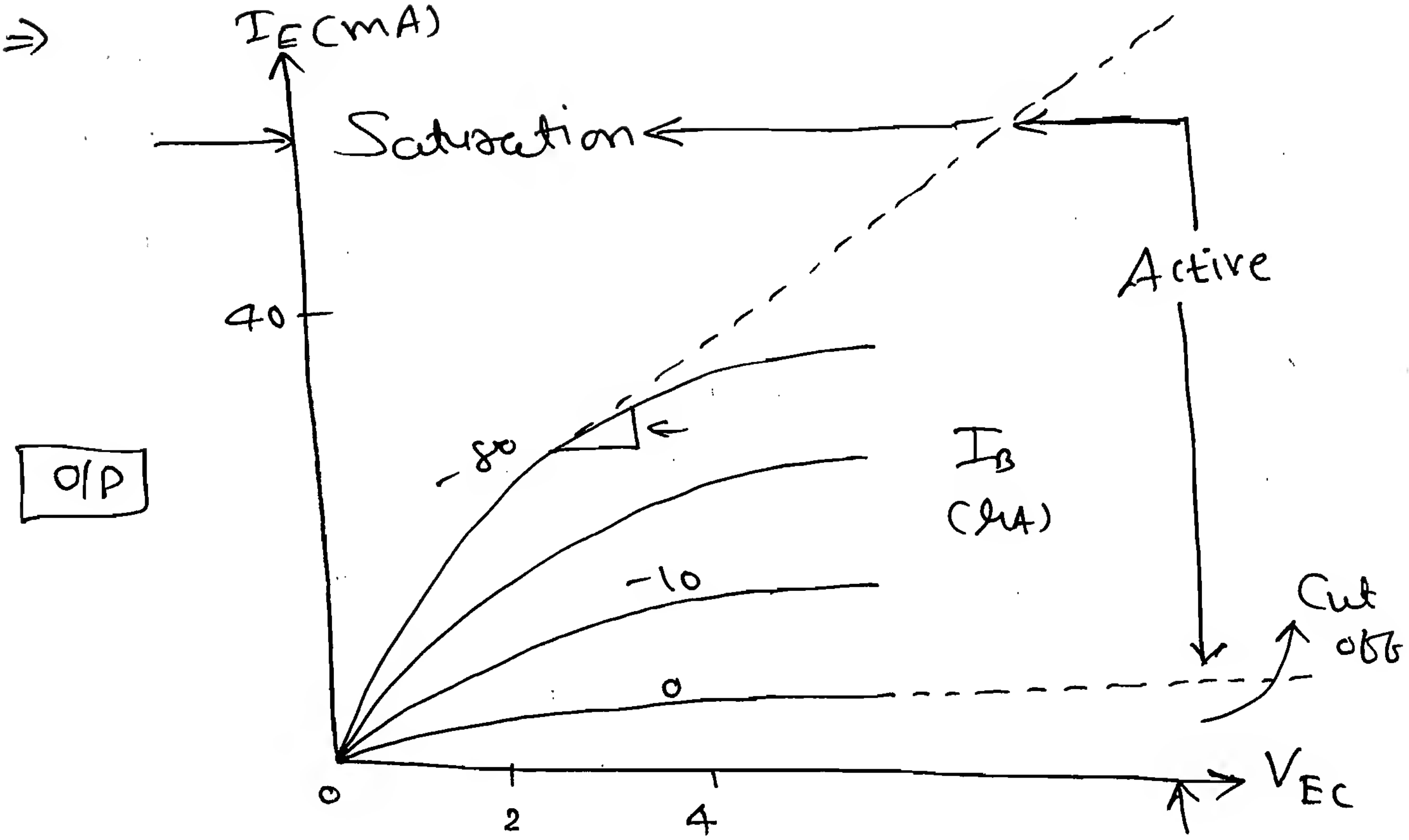


$$\Rightarrow \quad \gamma = (-I_E / I_B)$$

$$1+\beta = 1 + \frac{I_C}{I_B} = \frac{I_B + I_C}{I_B} = -\frac{I_E}{I_B} = \gamma.$$

	α	$<<$ β	$<$ γ
A_I :	CB	CE	CC
	(0.98)	(49)	(50)

⇒ γ : Common Collector forward current transfer ratio (or) CC current gain.

* <u>Input</u> <u>Characteristics:</u>

⇒ With V_{EC} kept constant if V_{BC} is increased then V_{EB}, Forward Biased to J_E decreases hence I_E & I_B decreases.

⇒ If V_{BC} further increases then V_{EB} further decreases and becomes less than V_r, Cut-in Voltage. hence I_E and I_B become '0'. i.e. I_B starts from a value decreases and finally becomes '0'. Hence input curves move up.

⇒ $$V_{EC} = V_{EB} + V_{BC} \longrightarrow V_{EB}\downarrow = \boxed{V_{EC}} - V_{BC}\uparrow$$

$$V_{EB}\downarrow \longrightarrow FB \text{ to } J_E\downarrow \longrightarrow I_E\downarrow \longrightarrow I_B\downarrow$$

$$V_{EB} < V_r \longrightarrow J_E \text{ not } FB \longrightarrow I_E = 0 \rightarrow I_B = 0.$$

* Output Characteristics:

⇒ Variable parameter in O/P of CE is same as CC but x-axis in o/p of CE is same as that of CC except for change in polarity.

⇒ y-axis in O/P of CE is same as that of CC except for slight increase in magnitude hence output of CC and CE look similar except that in CC slope is slightly greater than CE hence

current gain in CC is (γ) slightly greater than CE (β).

Q A typical BJT has a β of 100. If collector current is 1mA. Assuming active region find base and emitter currents.

Soln: $\beta = 100$, $I_C = 1mA$.

$$\therefore \beta = \frac{I_C}{I_B}$$

$$I_B = \frac{I_C}{\beta} = \frac{1mA}{100}$$

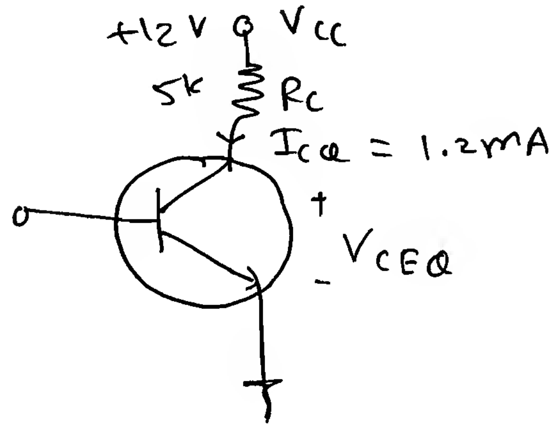
$$\therefore \boxed{I_B = 10\mu A}$$

$$\therefore I_E = I_C + I_B$$

$$\boxed{I_E = 1010\mu A}$$

$$\Rightarrow \boxed{I_E = 1.01mA}$$

Q for the BJT given in ckt determine Q-point.



$\therefore$ Sol^n:

$$\boxed{I_{CEQ} = 1.2mA}$$

$$\therefore \quad V_{CEQ} = V_C - V_E$$

but $V_E = 0$.

$$\therefore V_{CEQ} = V_C = V_{CC} - I_{CQ} \cdot R_C$$

$$V_{CEQ} = 12 - (5 \times 1.2).$$

$$= 12 - 6$$

$$\therefore \boxed{V_{CEQ} = 6\ V}$$

Q- Point : $(V_{CEQ}, I_{CQ}) = (6, 1.2mA)$.

$\boxed{Q}$ In grounded base configuration Voltage drop across a load resistor of 4 K is 3V. determine base current given $\alpha = 0.96$.

Sol^n:

$$\boxed{\beta = \frac{\alpha}{1-\alpha}}$$

$$I_C = 3/4 = 0.75mA.$$

$$\alpha = 0.96.$$

$$I_B = \frac{I_C}{\beta}$$

$$I_B = \frac{0.75}{24}$$

$$\therefore \beta = \frac{\alpha}{1-\alpha}$$

$$\beta = \frac{0.96}{0.04} = 24$$

$$\alpha = \frac{I_C}{I_E}$$

$$\alpha = \frac{I_C}{I_B + I_C}$$

$$\frac{1}{\alpha} = 1 + \frac{I_B}{I_C}$$

$$\frac{1}{\alpha} = 1 + 1/\beta.$$

$$\Rightarrow \boxed{I_B = 31.25\,\mu A.}$$

$$\boxed{I_E = I_C/\alpha = 0.781\,mA}$$

Q In a CB configuration emitter current is 1.6 mA, collector current with emitter open is 10 μA. Calculate collector current? given gain is 0.95.

Soln:

$$I_C = |-\alpha I_E| + I_{CBO}.$$

$$\therefore I_C = (0.95 \times 1.6) + 10\mu.$$

$$\Rightarrow \boxed{I_C = 1.53\,mA}$$

Q For CE mode BJT base current is 10 μA current gain 99. $I_{CBO} = 1\,\mu A$. Calculate collector current.

Soln: $I_B = 10\,\mu A.$

$$\therefore I_C = \beta I_B + I_{CBO}.(1+\beta)$$

$$= (99 \times 10\mu) + 1\mu\,(100).$$

$$I_C = 1090\,\mu A$$

$$\therefore \boxed{I_C = 1.09\,mA}$$

Q. For a BJT Collector current is 0.9 mA, Base current is 20 μA. Calculate α.

Soln:
$$I_C = 0.9\,mA$$
$$I_B = 20\,\mu A$$

$$\therefore \beta = \frac{\alpha}{1-\alpha}$$

$$\beta = \frac{I_C}{I_B}$$

$$\beta =$$

$$\beta(1-\alpha) = \alpha$$
$$\beta = (1+\beta)\alpha$$
$$\alpha = \beta / 1+\beta$$

$$\alpha = \frac{I_C}{I_E}$$

$$\alpha = \frac{0.9m}{0.9m + 20\mu}$$

$$\therefore \boxed{\alpha = 0.978}$$

Q. given common base current gain as 0.98. calculate CE current gain.

Ans:
$$\alpha = 0.98$$

$$\beta = \frac{\alpha}{1-\alpha}$$

$$\therefore \beta = \frac{0.98}{0.02}$$

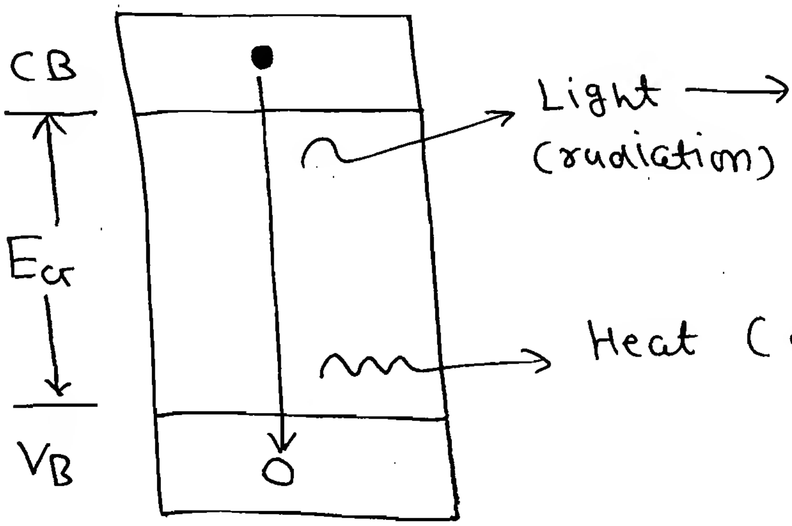
$$\boxed{\beta = 49}$$

☆ Opto Electronic Divices:

⇒ LED & LASER Convert electric energy to light energy and are used as optical Sources.

⇒ PIN & APD Convert light energy to electric energy and are used as optical detectors in fiber optic communications.

⇒



$\lambda(\mu m) = \frac{1.24}{E_G(eV)}$.

⇒ In certain semiconductors EHP Recombination occurs in two steps called Indirect transition (or) Indirect Recombination and E_G gets Converted to heat (dissipation). Such Semiconductors are called Indirect band gap Semiconductors. e.g. Ge (or) Si.

⇒ In some other semiconductor EHP recombination occurs in single step called direct transition (or) direct recombination and E_G gets converted to light (radiation) such semiconductors are called direct band gap semiconductors. e.g. Gallium (Ga) Arsenide (As).

⇒ If a P-N Junction is design using indirect Band gap Semi conductor and operated in F.B. then during recombination heat comes out called P-N diode.

⇒ If the same P-N junction is design using direct band gap semiconductor then during recombination light comes out called LED. The colour (or) wavelength emitted depends on E_G, ~~to~~ To produce required coloured as O/P. Two (or) more semiconductors are mixed to form a compound such that componds energy band gap is equal to required E_G.

⇒ Compound:

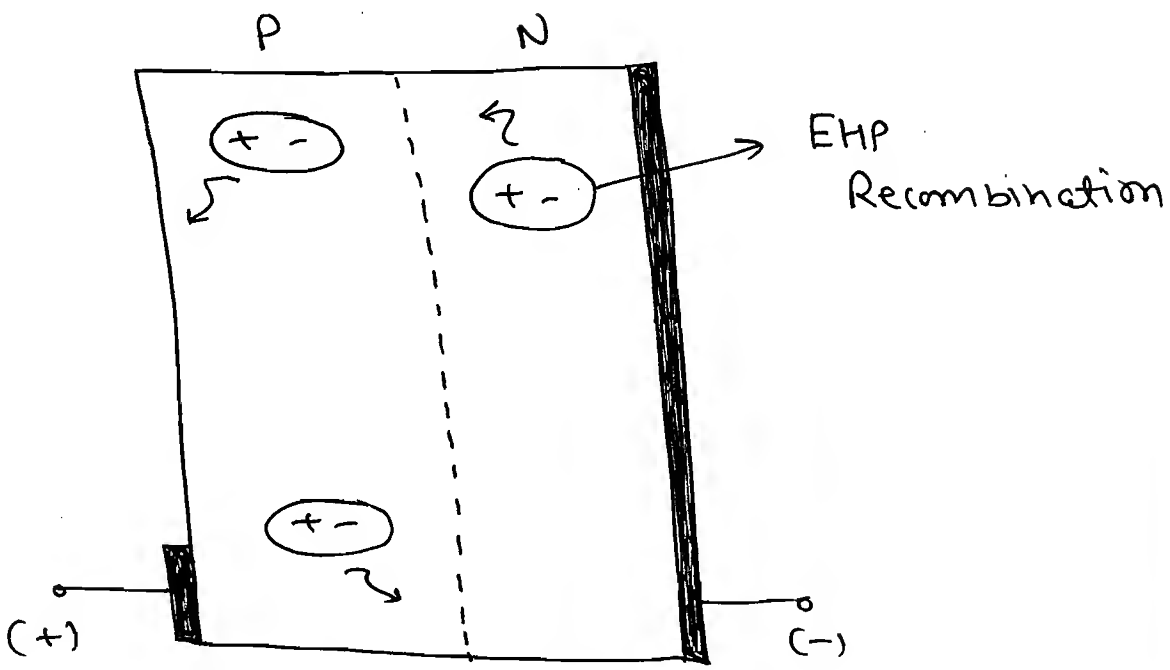
→ Binary : GaAs.

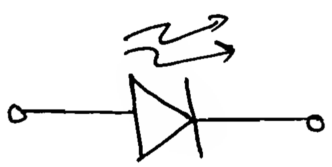
→ Ternary : GaAsP

→ Quarternary : InGaAsP.

* Light Emitting Diode (LED).

⇒





⇒ A P-N junction is design using direct band gap semiconductor and operated in FB condition then during EHP recombination Eg gets converted to light.

⇒ A two terminal device is emitting light hence called Light emitting Diode.

=> Applied electric field is responsible for light emission called <u>electroluminations.</u>

=> Injected charge carriers during recombination give out light called <u>injection luminations.</u>

=> During recombination light comes out called <u>radiative recombination</u>.

=> In p-N diode during recombination heat comes out called dissipative recombination.

=> In LED Spontenous Emission occurs.

* Advantages:

=> Small size
=> Less weight.
=> Low cost.
=> Long life.
=> Low power Consumption.
=> Rugged Construction.
=> Temp. depedence is less.

* Disadvantages:

=> Not highly directional.
=> Not highly cromatic.

* Light Amplification by Stimulated Emission of Radiation. (LASER).

⇒ If EHP recombination occurs after completion of life time and E_G gets converted to light then it is called spontenous emission which occurs in LED.

⇒ If recombination occurs before life time completion due to external disturbance and light comes out it is called stimulated emission which occurs LASER.

⇒ LASERs are produced in cavity. In a cavity say population inversion is achieved and an injected photon disturb an e^- and comes out as such the disturb e^- during recombination generates another photon hence one photon becomes two. The process repeates and due to light amplification voluminous photons are generated. Light is coming out due to

due to stimulated emission with light amplification hence called LASER.

* Advantages:

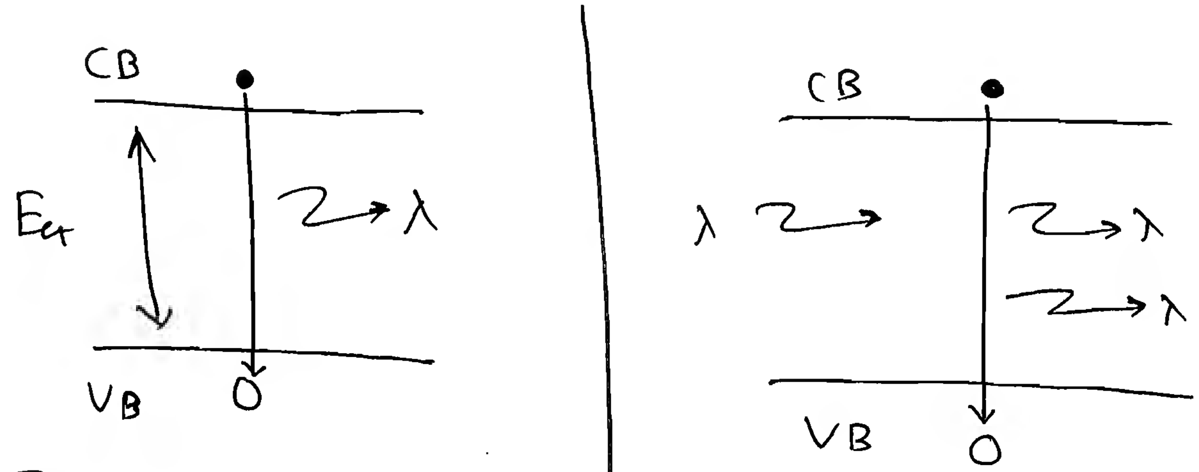
⇒ Highly directional.

⇒ Highly chromatic.

* Disadvantages.

⇒ (Invert the advantages of LED).

⇒

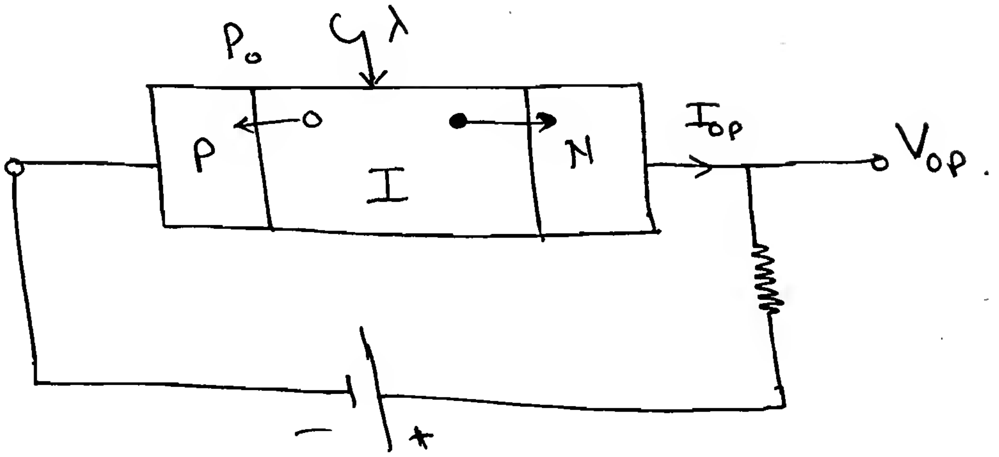


⇒ Spontaneous Emission

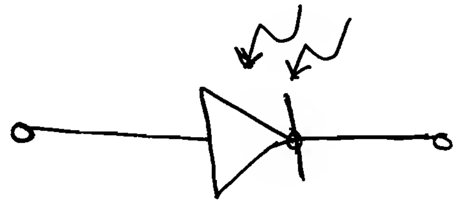
Stimulated emission

* PIN Photodiode:

⇒



⇒



⇒ $E_\lambda \geq E_G$

$$E_\lambda = hf = \frac{hc}{\lambda} \rightarrow \underset{(\mu m)}{\lambda_{max}} = \frac{1.24}{E_G(eV)}$$

⇒ Quantum efficiency → $\eta = \dfrac{\text{No. of EHP's generated}}{\text{No. of Photons Incidented}}$

$$\boxed{\eta = \frac{I_p/q}{P_o/hf}}$$

⇒ Responsivity $\boxed{R = \frac{I_P}{P_o} = \frac{\eta q}{hf}}$ Amp/WATT.

⇒ λ : Wavelength of incident photon.

f : freq. of incident photon.

P_o : Incedent optical power.

h : planck's constant.

→ C : Speed of light

I_p : photo current generated in PIN diode.

⇒ If a Photon having an energy greater than or equal to E_g of a semiconductor falls on the same semiconductor then by absorbing energy of photon. photo carriers are generated which get attracted towards opposite polarity of applied reverse biased and produced photo current I_p.

⇒ Light energy is converted to electric energy hence called photodiode. In the absense of light thermally generated charge carriers support reverse saturation current I_0 called Dark current.

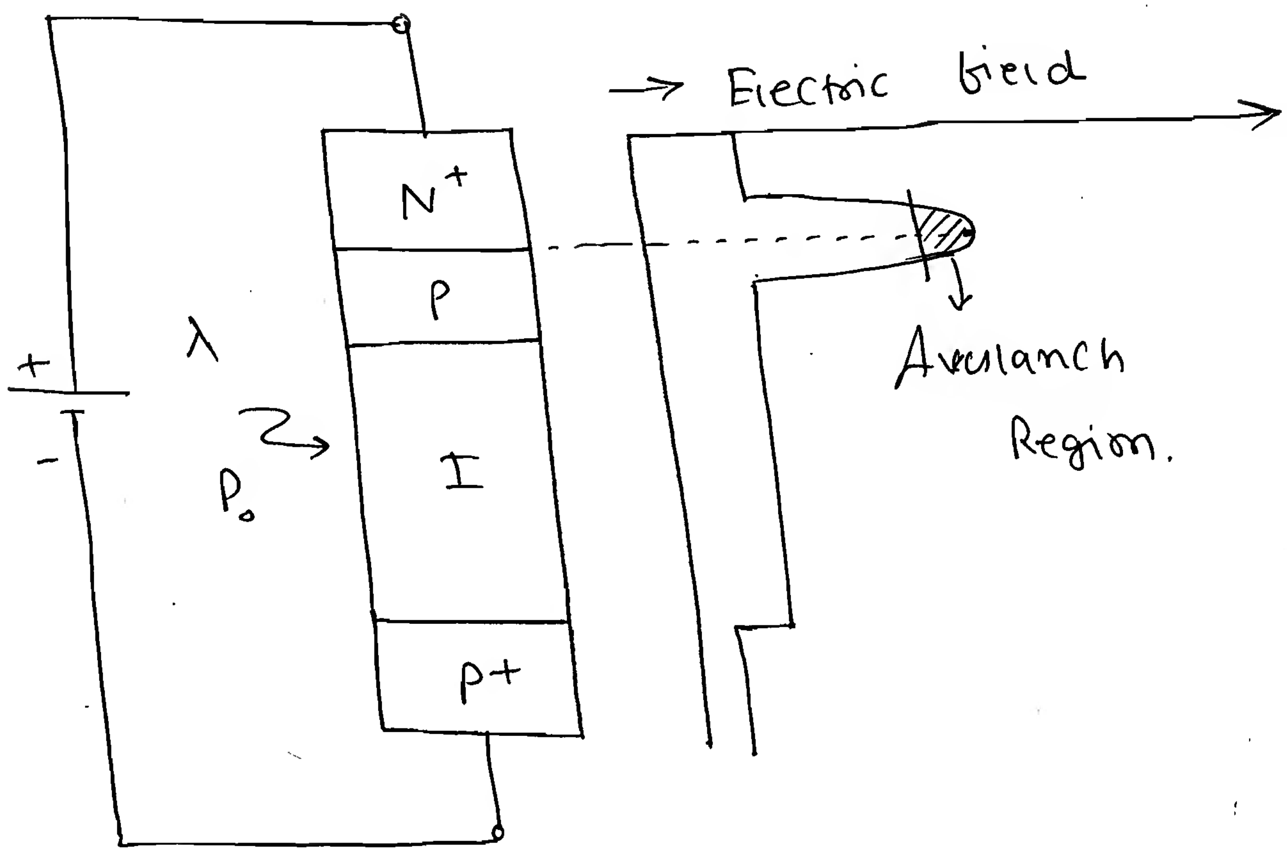
⇒ The range of wavelength over which photo diode gives output is called Spectral Response.

⇒ Minimum optical power to be incidented

on a photo diode to produce a usuble output is called light sensitivity.

* Avalanch Photodiode (APD):

⇒



⇒ $M = \frac{I_M}{I_p} > 1.$

$R_{APD} = \frac{\eta q}{hf} . M,$

⇒ M : Multipiication factor due to avalanch multipiication.

I_M : Multipiied photo current generated in APD.

⇒ due to incident photons photo carriers are generated which pass through n^+p jn where a large reverse external electric field is applied. due to which avalanch BD occurs. Hence avalanch multiplication starts. hence charge carriers and current increases.

⇒ For a power P_0 incident on APD say I_M is the current generated and for the same power incidented on PIN diode say I_p is the current generated then

$$\frac{I_M}{I_p} > 1.$$

⇒ Increase in charge carriers and current is called current amplification.

⇒ (a) A silicon APD has a quantum efficiency of 0.65 at a freq. of 0.33×10^{15} Hz. Suppose 0.5 μW of optical power produces a multiply photo current of 10 μA. Calculate the multiplication factor M.

$\underline{\text{Soln}}$:

$$\cancel{I_M} = \frac{\cancel{\eta q}}{\cancel{hf}} \cdot \cancel{M}$$

$$\Rightarrow \cancel{M} = \frac{\cancel{I_M \cdot hf}}{\cancel{\eta q}}.$$

$$\cancel{M} = \cancel{10 \times 10^{-6}} \times$$

$\Rightarrow$ Applied η and P_o to PIN diode and calculate I_p.

$$\therefore \quad I_p = \frac{\eta q}{hf} \times P_o.$$

$$\therefore \quad I_p = \frac{0.65 \times 1.6 \times 10^{-19}}{6.626 \times 10^{-34} \times 10^{15} \times 0.33} \times 0.5 \times 10^{-6}$$

$$I_p = 0.238 \, \mu A$$

$$M = \frac{I_M}{I_p} = \frac{10 \, \mu A}{0.238}$$

$$M = 42.05$$

$$\boxed{M \simeq 42.}$$

(a) A PIN photodiode is constructed with GaAs which has a band gap of 1.43 eV find the longest ~~wave~~ wave length that can generate current.

$\underline{\text{Soln}}$:

$$\lambda_{max} (\mu m) = \frac{1.24}{E_g (eV)}.$$

$\Rightarrow \quad \lambda_{max}(\mu m) = \frac{1.24}{1.43}$

$$\boxed{\lambda_{max} = 0.86\ \mu m}$$

Q 6×10^6 photons are incedent on a PIN diode and 5.4×10^6 EHPs are generated. Calculate Quantum efficiency.

Soln:

$$\text{Quantum efficiency } \eta = \frac{\text{No. of EHP's generated}}{\text{No. of incident photon}}$$

$$\eta = \frac{5.4 \times \cancel{10^6}}{6 \times \cancel{10^6}}$$

$$\boxed{\eta = 90\ \%}$$

Q Photons are incident on a PIN diode which has a responsivity of 0.65 A/watt. If optical power level is $10\ \mu W$. Calculate photo current generated

Soln:

$$I_p \neq R/q \qquad \frac{I_p/q}{P_0/h\nu}$$

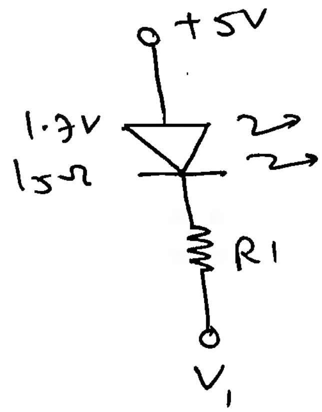
$$R = \frac{I_p}{P_0}$$

$$\therefore \quad I_p = R.P_0 = 0.65 \times 10 \times 10^{-6}$$

$$\boxed{I_p = 6.5\ \mu A}$$

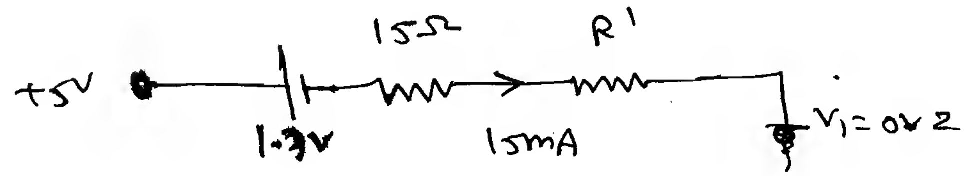
(a) A LED is connected as shown it should glow when V_1 is at logic '0' state (0.2V). Calculate R'. Assume in active state current as 15 mA.

Sol^n:



$\Rightarrow$ V_1 is at Logic '0' $\Rightarrow$ $V_1 = 0.2 = 0.2$

∴



∴ By KVL,

$$5 - 1.7 - 0.2 - (15 + R')\,15m = 0.$$

$$\frac{3.1}{15} = 15 + R'.$$

∴ $\boxed{R' = 191.67\ \Omega}$

* Junction Field Effect Transistor (JFET):

=>

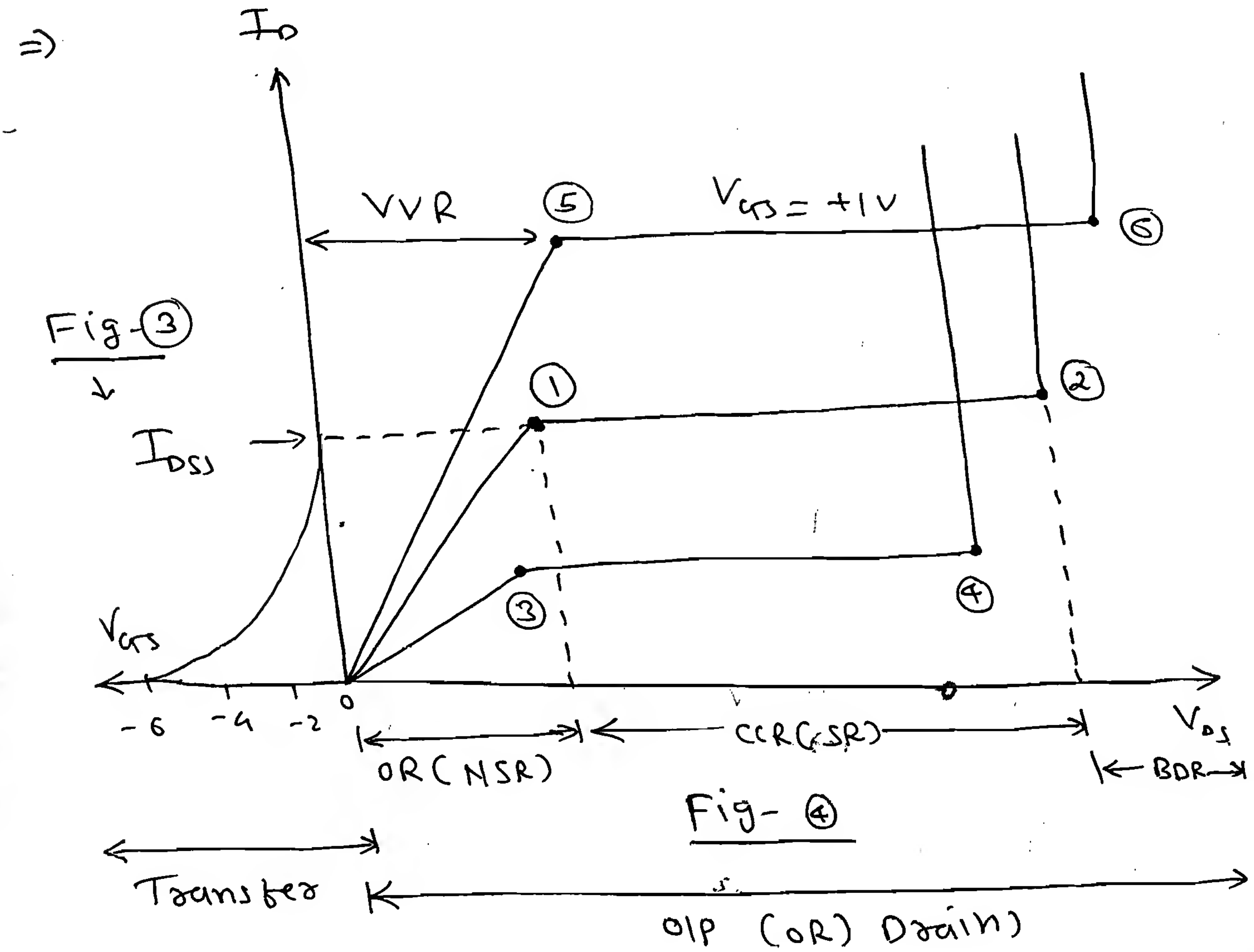


Fig-③

Fig-④

=>

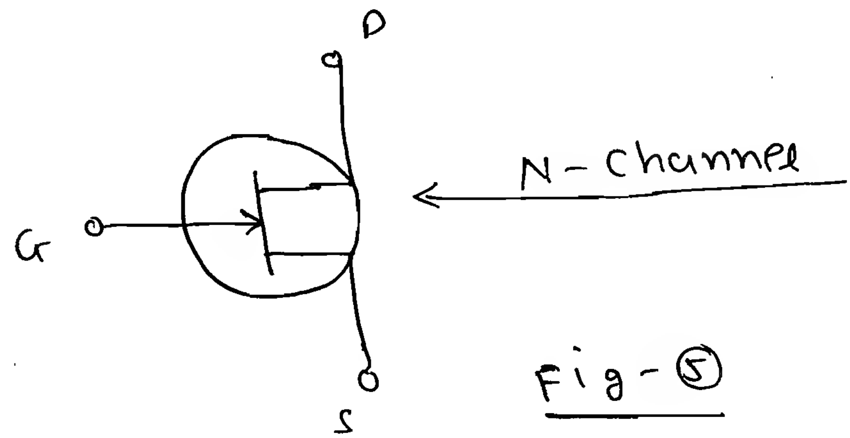


Fig-⑤

=>

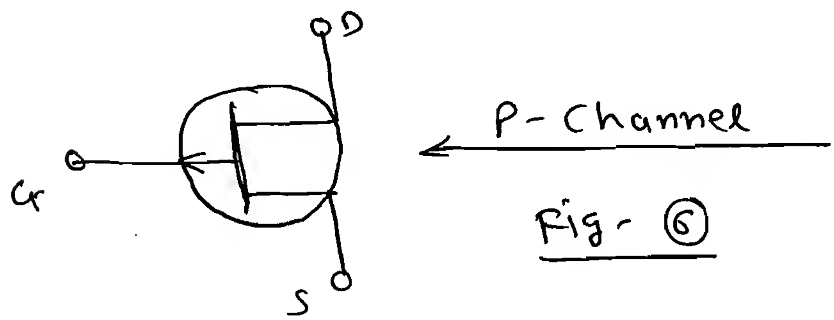
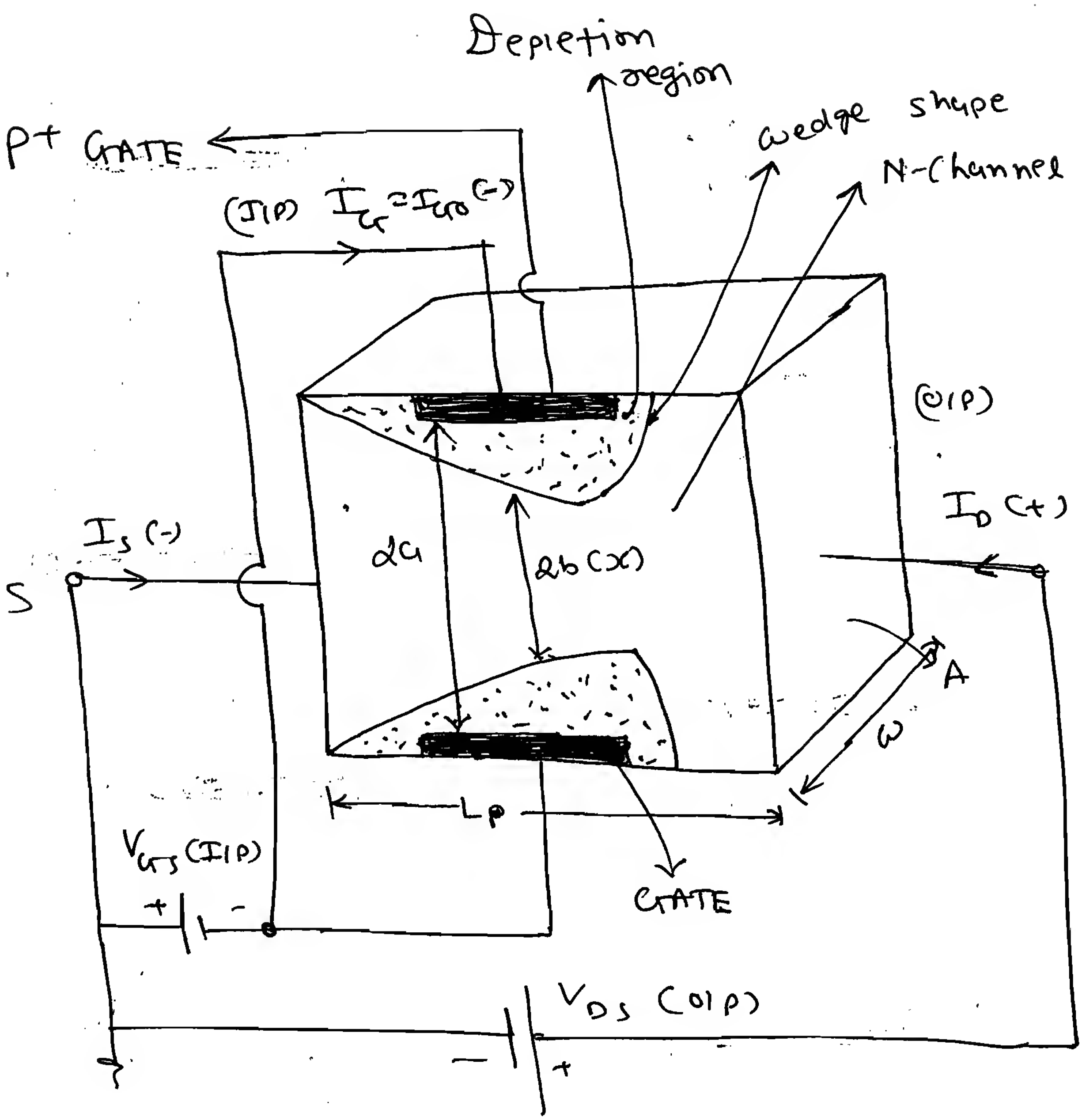


Fig-⑥

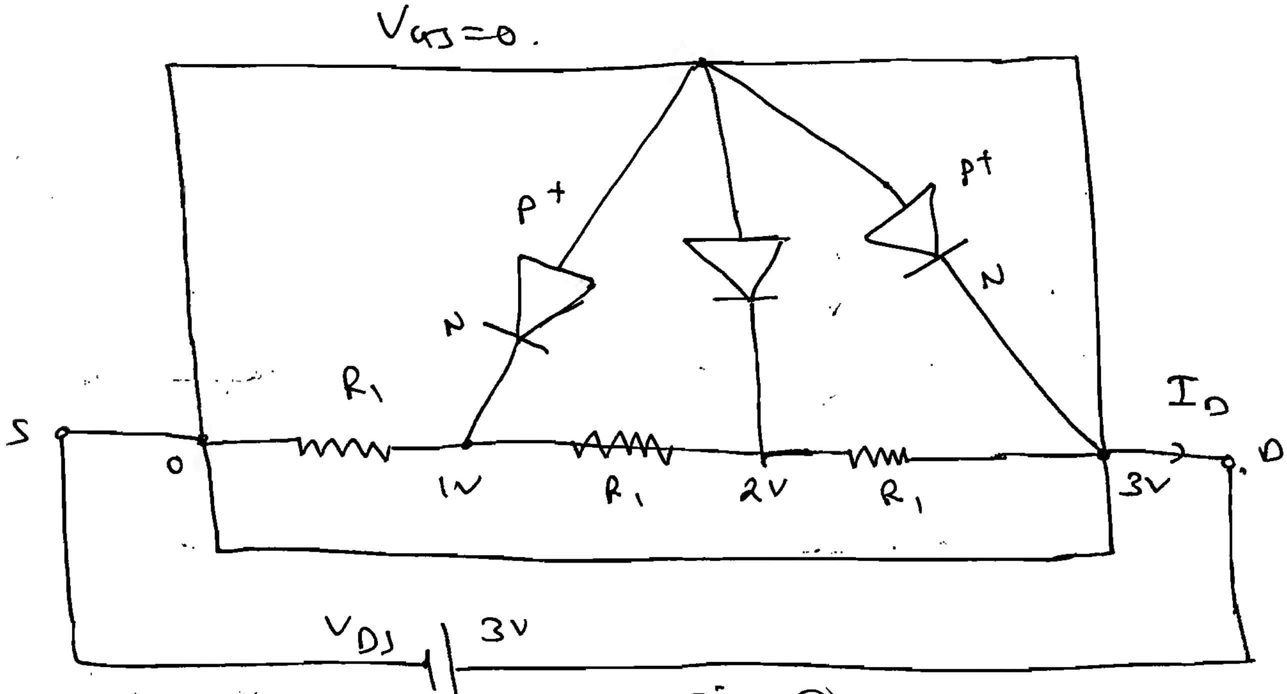
=>



Depletion region
wedge shape
N-Channel
P+ GATE
(I/P) $I_G = I_{GO}$ (-)
(O/P)
I_D (+)
I_S (-)
S
2a
2b(x)
A
W
L
GATE
V_{GS} (I/P)
+ -
V_{DS} (O/P)
- +

Fig- ①

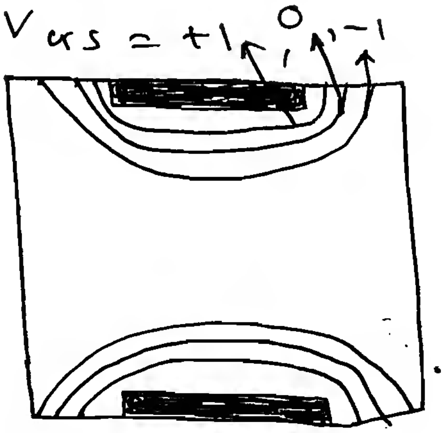
=>



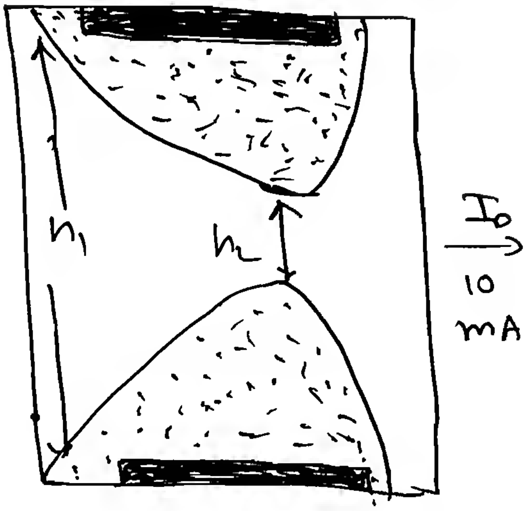
$V_{GS} = 0$.
P+
N
P+
N
R_1
R_1
R_1
S
0
1V
2V
3V
I_D
D
V_{DS}
3V
- +

Fig-②

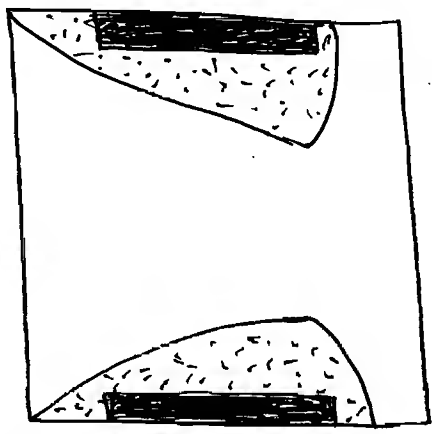
Ⓐ $V_{DS} = 0$



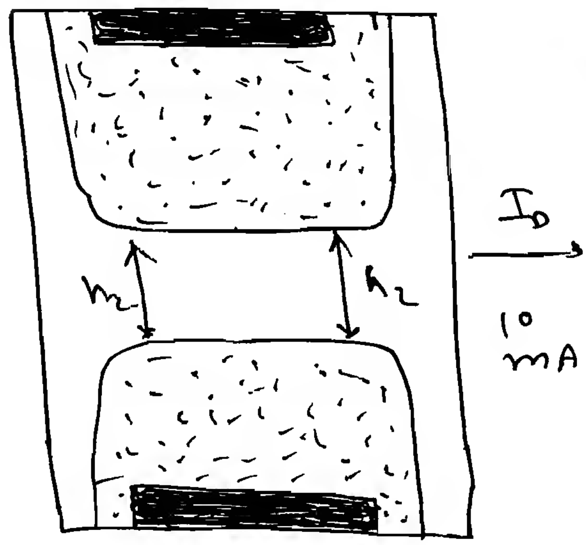
Ⓒ $V_{DS} \uparrow\uparrow$ (6V)



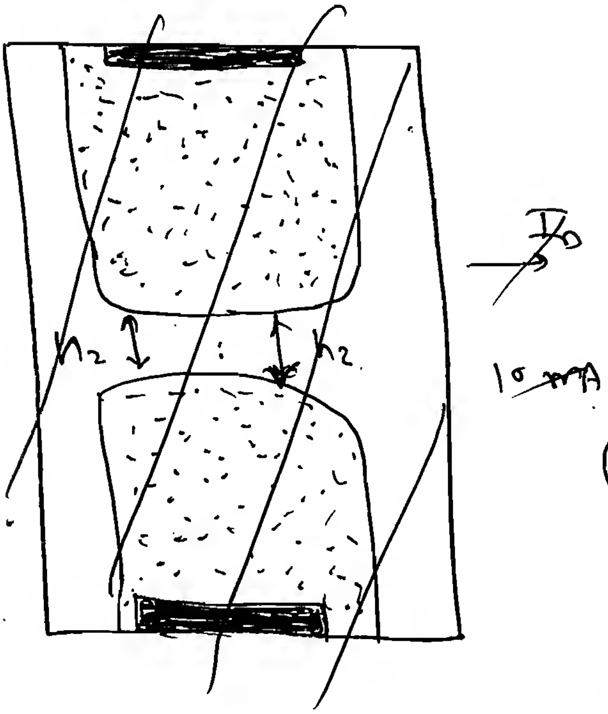
Ⓑ $V_{DS} \uparrow$ (3V)



Ⓓ $V_{DS} \uparrow\uparrow\uparrow$ (10V)



~~Ⓔ~~



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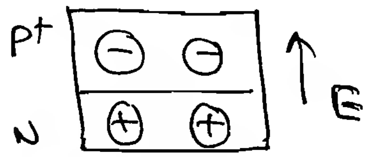
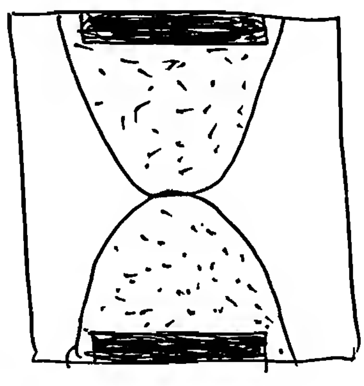


Ⓔ

$V_{GS} \uparrow\uparrow$ (-6V)



⇒ Channel supports flow of only one charge carrier hence it is unipolar device.

⇒ The voltage betn drain and source V_{DS} is to be choosen such that charge carriers enter through source terminal into channel and leave the channel through drain terminal.

⇒ The Top and Bottom p+ gates along with n-channel form gate junction diodes.

⇒ The voltage betn gate and source V_{GS} is to be choosen such that gate junction diodes are reversed biased.

⇒ Interchanging drain and source terminal will not affect the operation hence circuit symbol doesn't differentiate betn drain and source terminals.

⇒ The direction of arrow shows the direction flow of current when gate jn diode is forward bias.

⇒ **Pinch- OFF:**

	V_{DS}	V_{GS}	I_D
①	↑	Const.	Const. (OR) (pinch off region)
②	Const.	↑	0

→ In fig - Ⓐ, the top and bottom curves drawn for $V_{GS} = 0$ and $V_{DS} = 0$ correspond to penetration of depletion region into channel under open circuit condition of gate jn diode.

→ ~~In~~ N- Channel, semiconductor bar acts like resistor across which a Voltage V_{DS} is given through which a current I_D flows.

→ As V_{DS} increases I_D increases linearly as shown in ohmic Region (OR).

→ From left to right length (L) increases Resistance increases, Voltage drop increases and Reverse bias given to n- side Progressively increases hence penetration

of depletion region into channel progressively increases hence depletion region takes an non-uniform shape called wedge shape.

→ To the left, to middle and right sides penetration of depletion region into channel will be more in $V_{DS}=$ 6V case than $V_{DS} = 3V$ case. since in 6V case reverse bias is more than corresponding 3V case but the shape is still non-uniform.

⇒ 2a: Height of channel. (distance betn gates)

a: Half height of channel.

2b(x): Effective height of channel (distance betn depletion region at a distance of x).

b(x): Effective half height of channel.

h_1, h_2: max, min effective height of channel.

→ minimum effective e. height decides the magnitude of drain current.

⇒ w.r.t. Stability and retaining of current fig - (D) is correct and fig - (B) is wrong hence as V_{DS} increases from 6V to 10V fig - (C) moves to (D) hence I_D becomes constant as shown in CCR (constant current Region).

⇒ Beyond CCR as V_{DS} increases across top and botton depletion region a large electric field gets developed and avalanch BD occurs hence avalanch multiplication starts hence charge carriers and I_D increase ~~or~~ uncontrollably as in BD region (BDR).

⇒ Maximum controllable current is possible in CCR hence called Saturation Region (SR). Hence OR (ohmic region) becomes Non Saturation

region (NSR).

→ ECR and VVR will occur at a lesser value of V_{DS} for $V_{GS} = -1V$ compare to $V_{GS} = 0V$ since in $V_{GS} = -1V$ case initial depletion region is deeper than $V_{GS} = 0V$ case. Device can be used as Voltage variable Resistor (VVR) by varying V_{GS} in ohmic region.

→ Input Resistance

$$R_{GS} = \frac{V_{GS}}{I_G}$$ is high.

⇒ As V_{GS} increases (more -ve) reverse bias given to gate in diodes increases more and more hence penetration of depletion region into channel increases hence minimum effective height and drain current decreases more and more. at a perticular Voltage fig-(E) occurs hence minimum effective height and I_D become zero. Thus, Transfer char. can be explained.

Note:

→ If V_{DS} increases and fig- E occurs then minimum effective height, drain current, current through Resistance, drop across Resistances and Voltage given to n side of diodes become zero hence the diodes are open circuited hence width of depletion region decreases hence fig- E jumps to A hence fig E earlier was unstable.

→ If V_{GS} increases and fig- E occurs then even if voltage given to n-sides of diodes becomes '0' still the diode are reversed biased due to -ve supply given by V_{GS} to p^+ side.

→ In a Reverse bias diode a large depletion region can survive hence this time fig- E is a stable state.

→ Pinch off voltage V_p is defined as Voltage betn gate and source V_{GS} for $V_{DS} = 0$ at which channel closes.

(V_p is -ve for n-Channel and +ve for p Channel).

→ As input Voltage V_{GS} increases, input Current I_G is Constant but output ~~Volta~~ Current I_D decreases hence it is Voltage ~~Constant~~ control device.

→ In Fig-(F), +ve means +very Charged donor ion existing in depletion region of n- Channel, -ve means -very Charged Acceptor ion existing in depletion region of p+ - gate.

→ Across +ve and -ve ions existing in depletion region internally electric flux line get developed which control the operation hence called electric field effect.

⇒ Electric field deloped across a junction is controlling the operation of a 3-terminal device hence called Junction Field Effect Transistor (JFET).

* Salient Points of JFET: (compare to BJT).

⇒ Voltage controlled device.

⇒ I/P Resistance is high.

⇒ No offset Voltage.

⇒ Unipolar device.

⇒ Small in size.

⇒ Better thermal Stability.

⇒ Easy to fabricate.

⇒ Low power Consumption.

Note:

→ In a BJT in the path of flow of current a junction exist hence a minimum offset voltage V_r to be applied for BJT to go to on state No such junction (or) offset voltage for JFET.

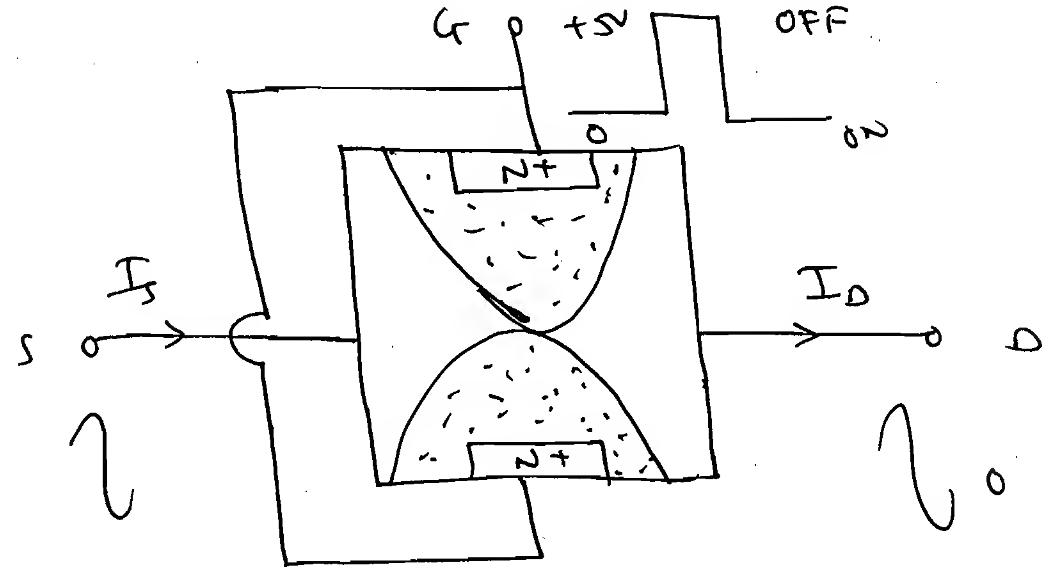
* Applications:

⇒ Voltage Variable resistor.

⇒ Buffer.

⇒ Digital Analog switch.

→ A digital pulse is controlling a operation of analog switch hence called digital analog switch.



⇒ $V_p = \left(-qN_D a^2/2\epsilon\right) \rightarrow$ N- Channel.

$V_p = \left(+qN_A a^2/2\epsilon\right) \rightarrow$ P- Channel.

$$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2.$$

→ $V_{DS} + V_p = V_{GS}.$

→ $V_{GS} = (1 - b/a)^2 V_p.$

→ $$I_D = \frac{2awqN_D\mu_n}{L}\left[1 - \left(\frac{V_{GS}}{V_P}\right)^{1/2}\right] V_{DS}.$$

$$r_{d,ON} = \left.\frac{V_{DS}}{I_D}\right|_{V_{GS}=0} = \frac{L}{2awqN_D\mu_n}.$$

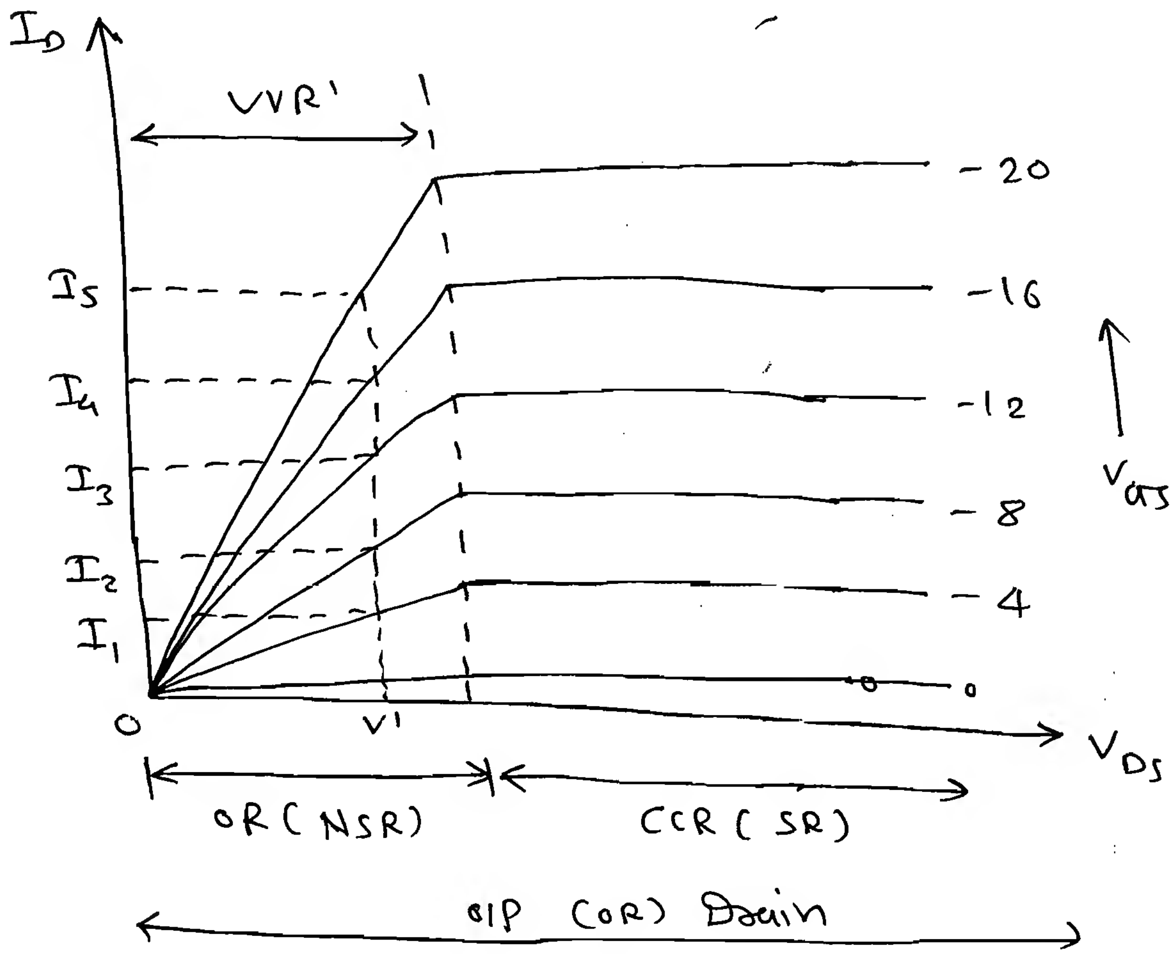
⇒ I_{DSS} : Drain saturation current at $V_{GS}=0$

I_{DS} : Drain satⁿ current when $V_{GS} \neq 0$.

$r_{d,ON}$: drain ON Resistance.

* Induced P- Channel Enhancement MOSFET (IGFET) (OR) PMOS.

⇒



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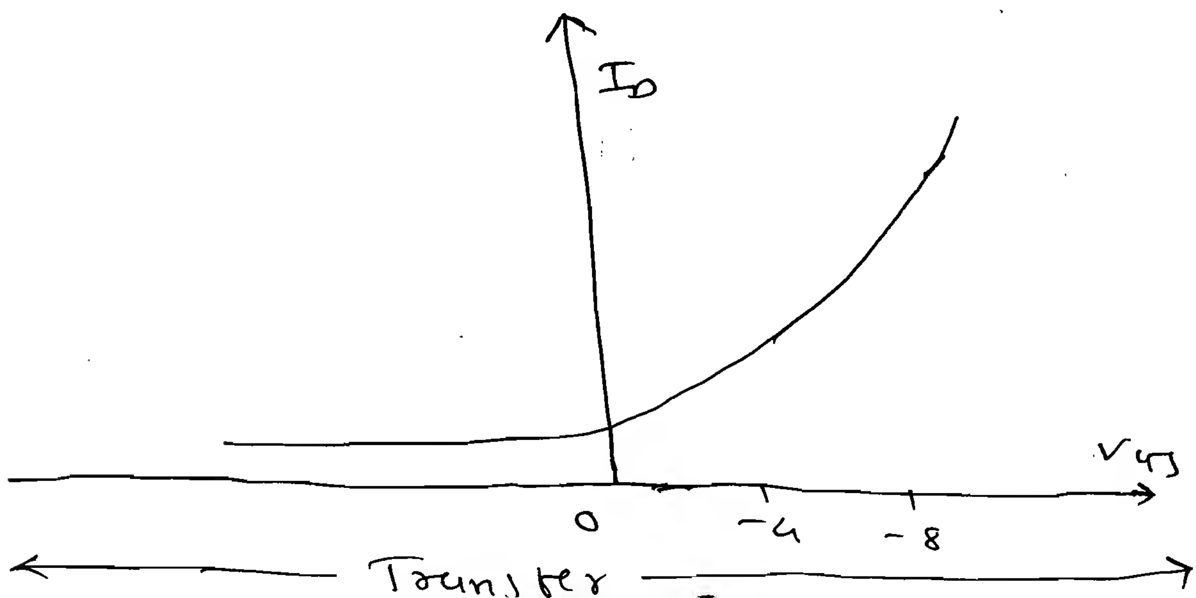

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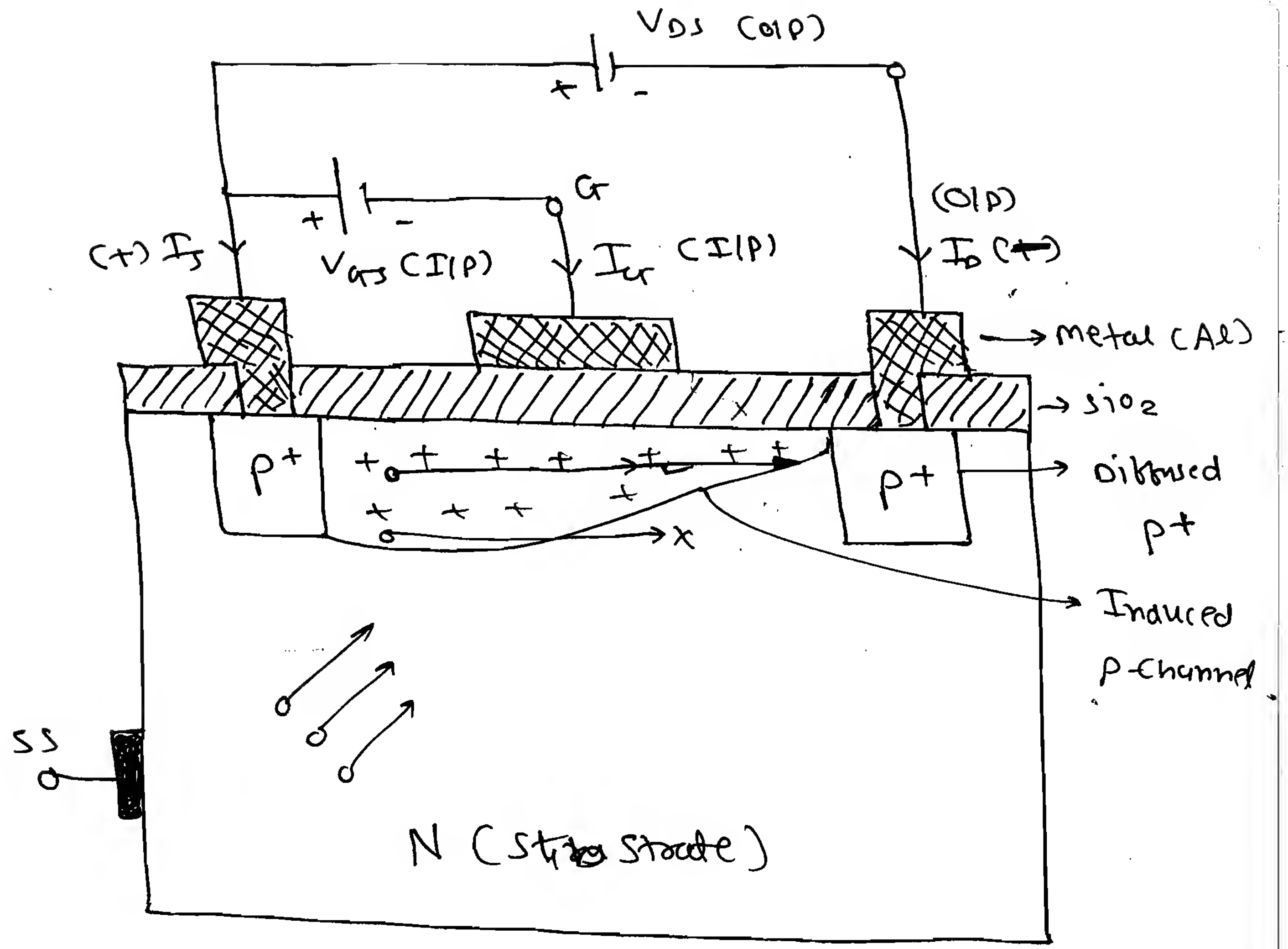
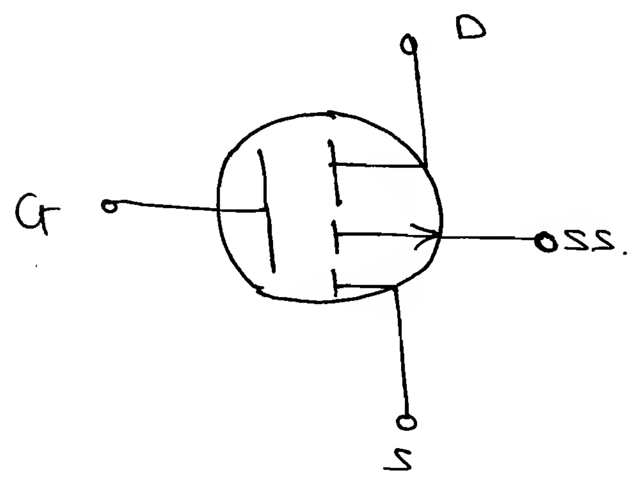


VDS (O/P)
G
(+) IS
VGS (I/P)
IG (I/P)
(O/P)
ID
metal (Al)
SiO2
p+
p+
Diffused p+
Induced p-channel
SS
N (Substrate)

⇒

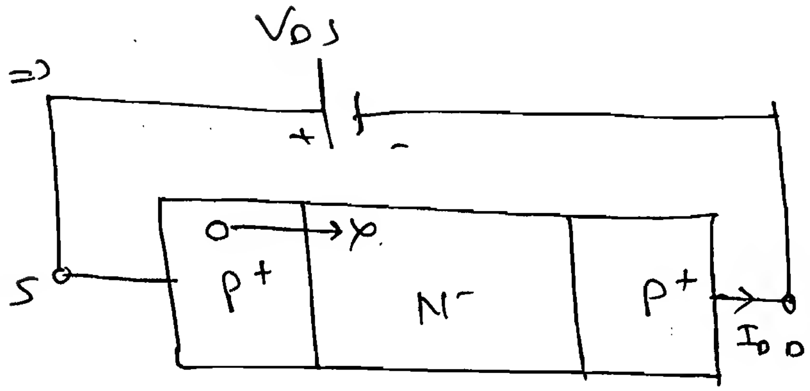


D
G
SS.
S

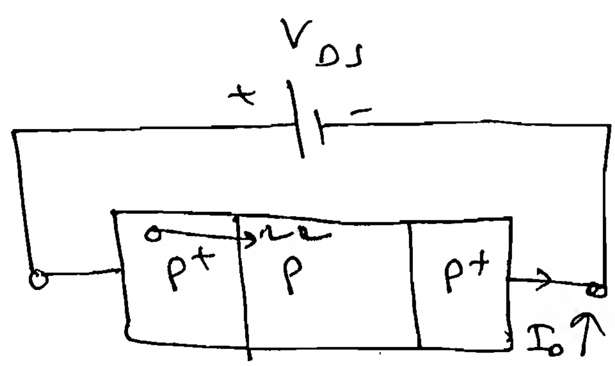
$V_{GS}=0$

$V_{GS}=-ve$

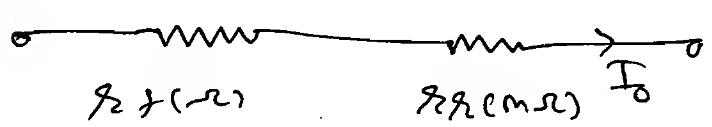
⇒



VDS
S
p+
N-
p+
ID



VDS
p+
p
p+
ID



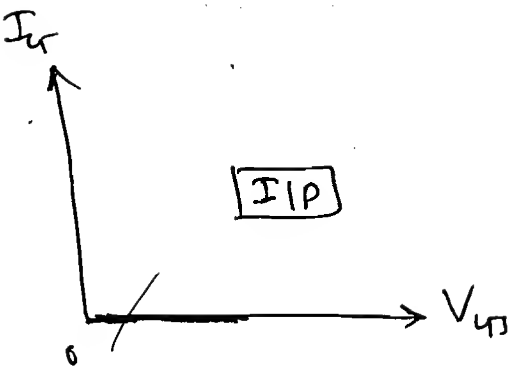
ID

⇒ $V_{DS} = V_{DG} + V_{GS}$

$V_{DS} = -V_{GD} + V_{GS}$

$V_{GD}\downarrow = \boxed{V_{GS}} - V_{DS}\uparrow$

⇒ $R_{GS} = \dfrac{V_{GS}}{\underset{\approx 0}{I_G}} = \infty .$



$R = \dfrac{\rho l}{A}$

$\uparrow V_{DS} = \uparrow I_D R$

⇒ Device supports flow of only one charge carrier hence ~~it~~ is unipolar device. The voltage betn D & S V_{DS} is to be choosen such that charge carriers enter through source terminal into device and leave the device through drain terminal.

⇒ For $V_{GS} = 0$ diffused p^+ region and n^- substrate form diodes. For a given V_{DS} source diode is forward bias and Drain diode is RB. hence $I_D = I_0$, very small current flows.

⇒ Even if V_{DS} increases $I_D = I_0$ will be

constant since n^- channel opposses the flow of charge carrier.

⇒ Sun V_{GS} is made -ve then holes of substrate are pulled towards gate terminal but they can ~~not~~ reach gate due to insulating SiO_2 layer hence they gete accumulated beneath SiO_2 layer betn the two p^+ region called Induced p- channel. which supports flow of charge carriers hence drain current increases.

⇒ For the same V_{DS} as earlier if V_{GS} becomes more and more -ve then channel becomes more and more p-type. hence I_D increases called Enhancement type.

⇒ For a given value of V_{GS} Induced channel and diffussed areas act like a resistor across which a voltage V_{DS} is given through which a current I_D flows as V_{DS} increases I_D increases linearly as shown in ohmic region ~~(OR)~~ (OR)

→ Beyond a Perticular V_{DS} if V_{DS} further increases Pull exrted on the incoming holes to the drain side decreases hence holes get accumulated at source side hence height of induced channel at drain side becomes constant hence I_D becomes constant as in constant current region (CCR). maximum current is possible in CCR hence called Saturation region (SR). and hence (OR) becomes non-saturation region (NSR).

⇒ Device can be used as Voltage Variable Resistor (VVR) in OR. by Varying V_{GS}.

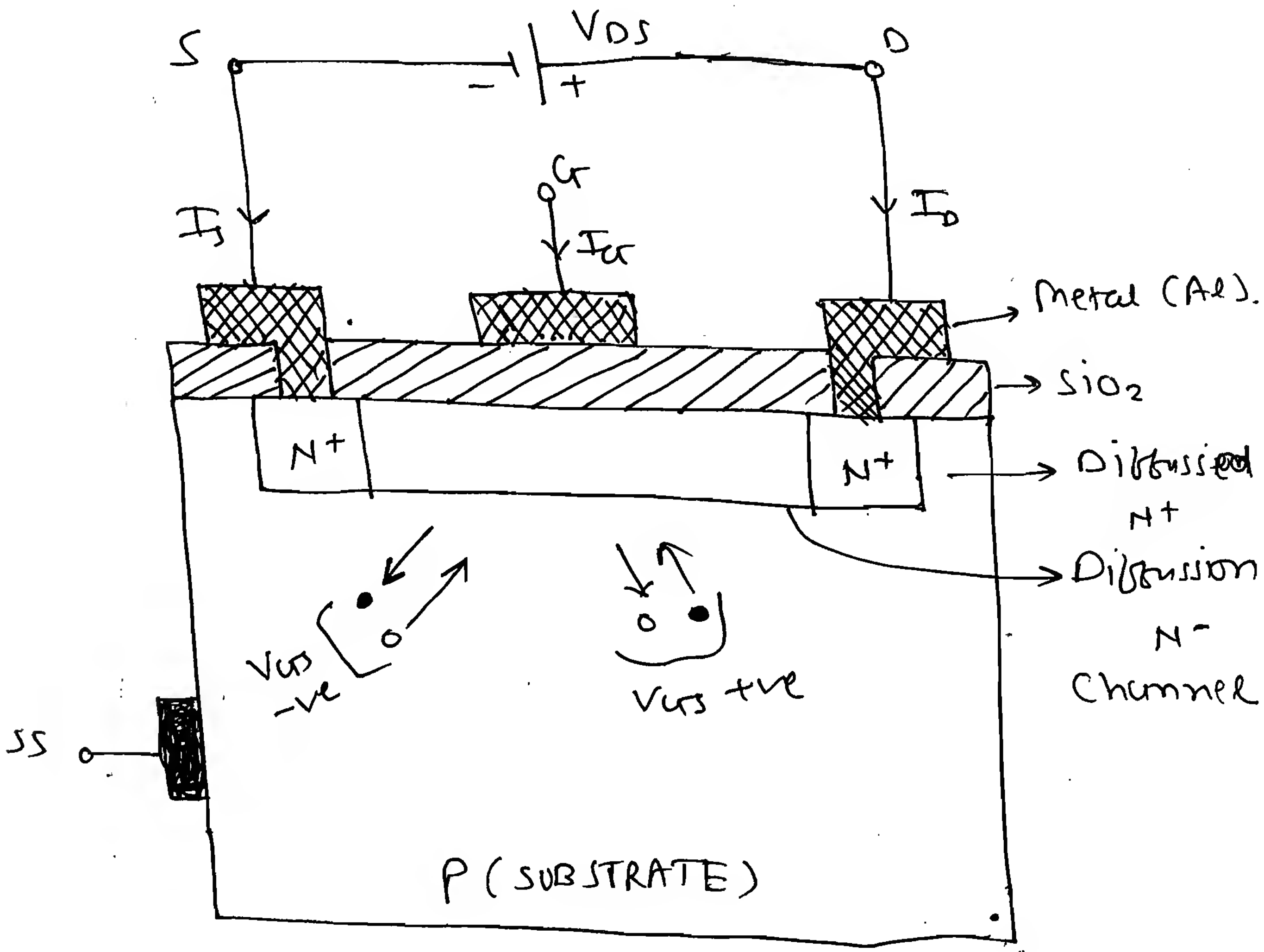
⇒ Input resistance $R_{GS} = \frac{V_{GS}}{I_G}$ ideally is infinity practically very high. since gate terminal is insulated by SiO_2 layer. As V_{GS}, ~~increases~~ input voltage increases input current I_G is constant and output current I_D increases hence It is Voltage Controlled Device.

⇒ Electric field devloped across Metal oxide semiconductor (MOS) is Controlling the operation of a 3-terminal device hence called Metal oxide semiconductor Field Effect Transistor. (MOSFET).

⇒ Gate terminal is Insulated hence called insulated gate field effect Transistor. (IGFET).

* Enhancement cum Depletion N-Channel MOSFET:

⇒



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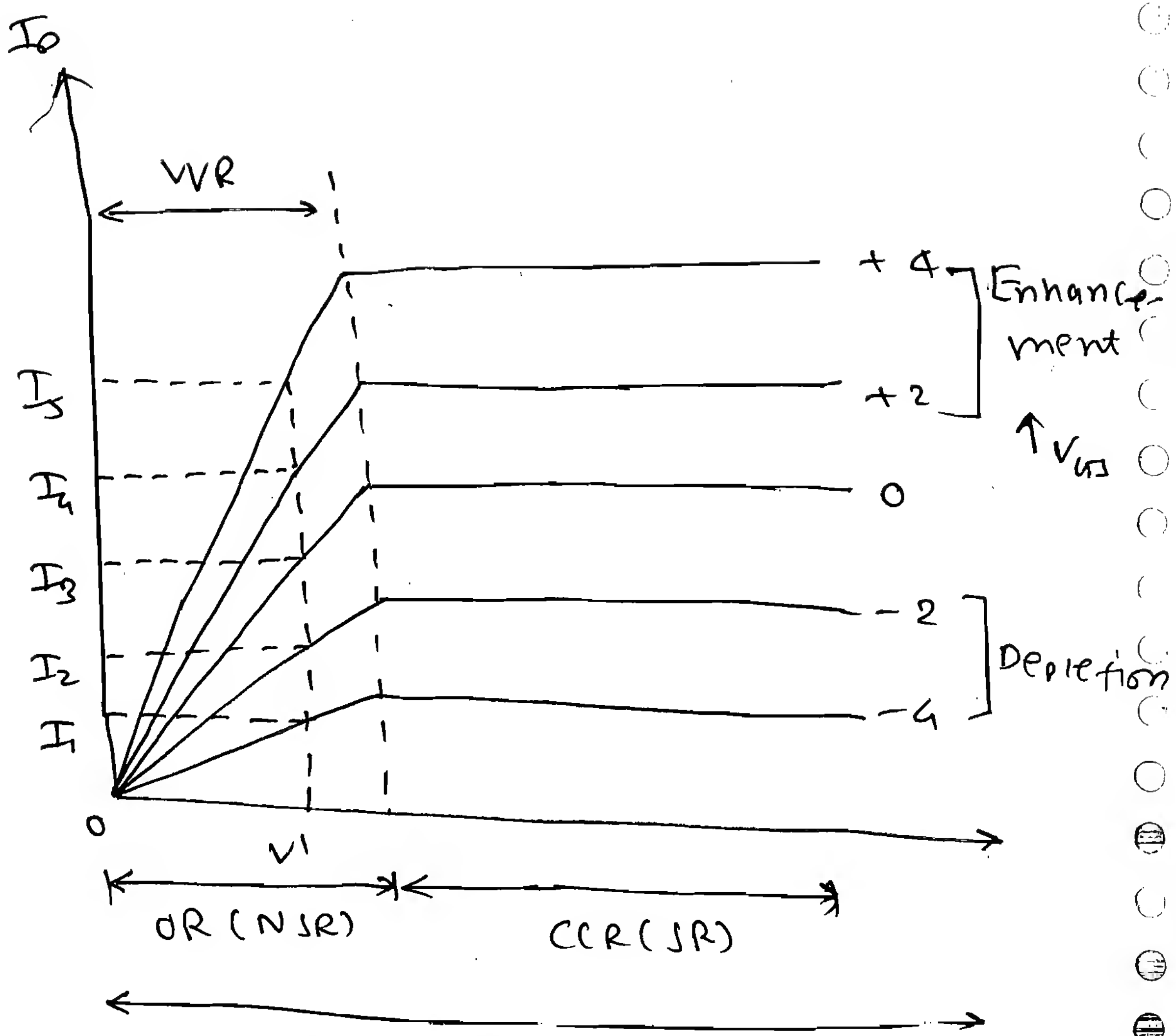
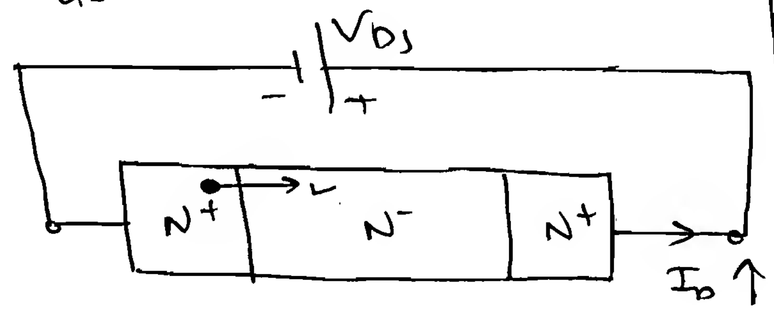


O/P (OR) Drain

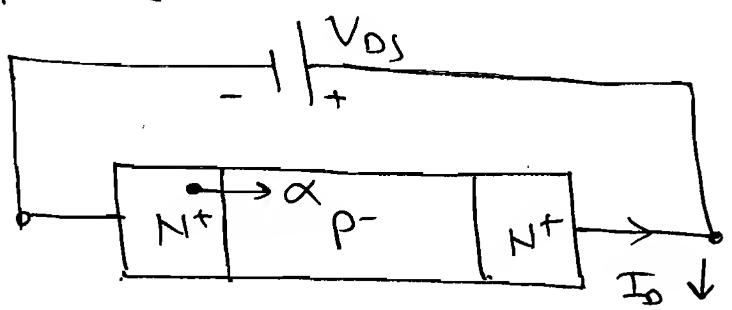
$V_{GS} = 0$

=)



$V_{GS} = -ve$

=)



$V_{GS} = +ve$

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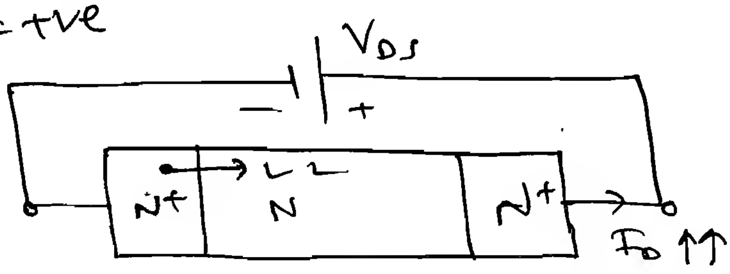
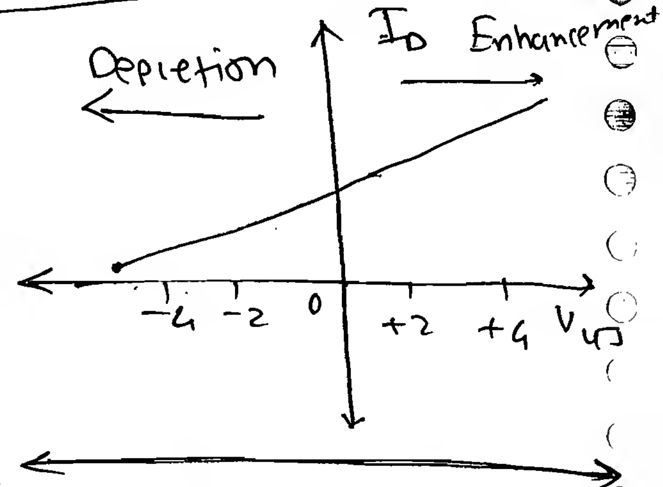
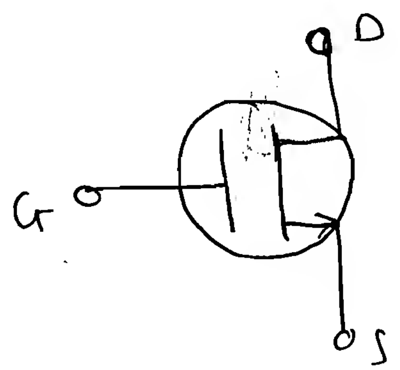




Transfer



⇒ For $V_{GS}=0$, diffussed n- channel supports flow of charge carrier hence, a non-zero value of I_D is possible.

⇒ Say V_{GS} is made -ve then e^- of channel are ripped to substrate and holes of substrate are attracted to channel hence channel becomes p-type and opposses flow of charge carriers hence I_D decreases called depletion mode.

⇒ Say V_{GS} is made +ve then holes of channel are ripped to substrate and e^- of substrate attracted into channel hence channel becomes more n-type hence I_D increases called Enhancement mode.

* Applications:

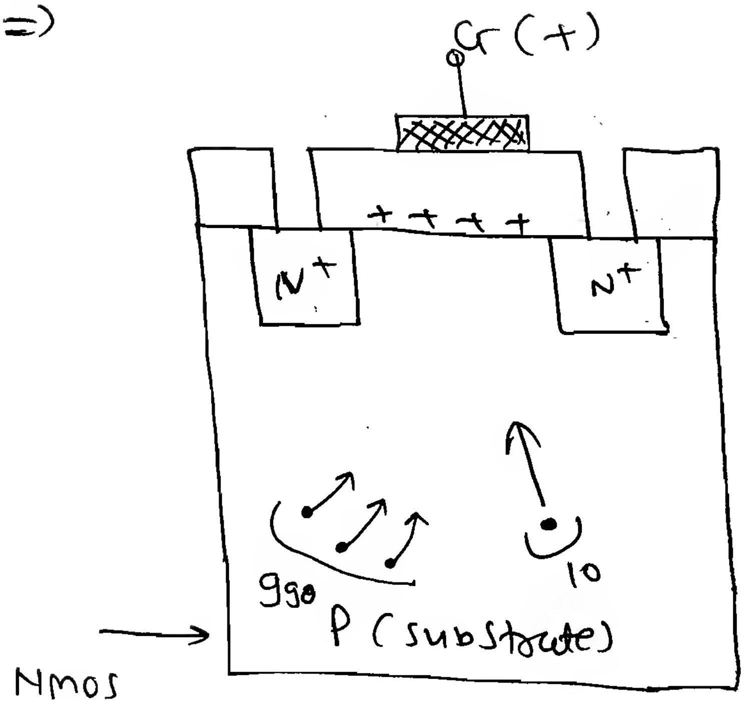
⇒ Voltage variable Resistor.

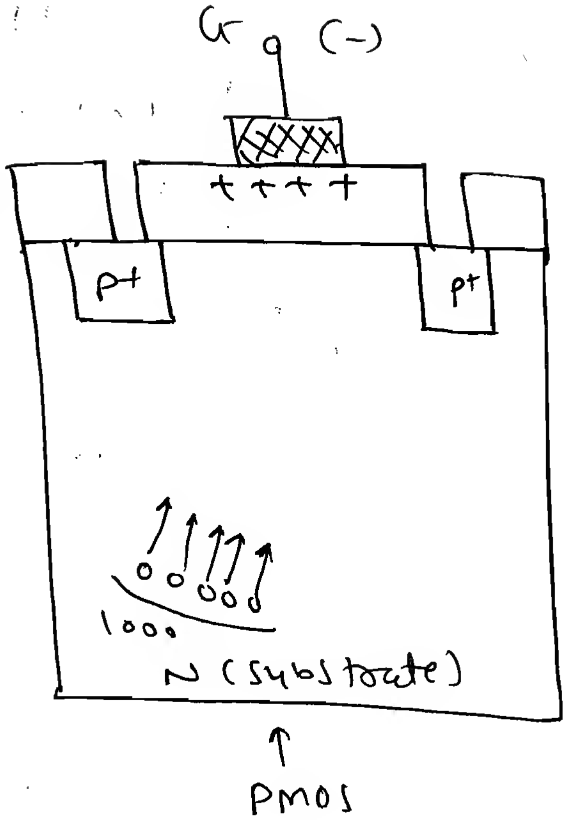
⇒ Buffer.

⇒ Memory element.

Note: In PMOS there is no ~~[illegible]~~ 'Premature ON' Problem

=)





$V_{GS} = +5V$

$V_{GS} = +4.9V$

$V_{GS} = -5V.$

"Premature ON"

=) During the preparation of SiO_2 layer certain +vely charge impurities will get developed which where seen to effect the operation.

=) In NMOS V_{GS} +ve will ripple the impurities hence they move the bottom surface of SiO_2 layer. and attract charge carriers into channel and make the device to get switched ON at a voltage prior to designed voltage called 'premature ON'' problem.

⇒ In PMOS V_{GS} -ve attracts impurities hence they move to top surface of SiO_2 layer. They can not affect incomming charge carriers hence device gets switched on at designed voltage.

Q An n-channel JFET has $I_{DSS} = 8mA$ $V_{GS(OFF)} = -5V$. Calculated minimum voltage betn D & S for pinch off. and drain current given $V_{GS} = -2V$.

Soln:

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2.$$

$$V_P = V_{GS(OFF)} = -5V.$$

$$\therefore \quad I_D = 8\left[1 - \frac{(-2)}{(-5)}\right]^2.$$

$$\boxed{I_D = 2.88mA}$$

$$\therefore \quad V_{DS} + V_P = V_{GS}$$

$$V_{DS(min)} = V_{GS} - V_P$$

$$= -2 - (-5).$$

$$\boxed{V_{DS(min)} = +3V}$$

$\boxed{Q}$ Gate current is 1 nA when a reverse gate voltage of 12 V is applied to a FET. R_{GS} (in) in MΩ is.

$\underline{\underline{\text{Soln:}}}$

$$R_{GS} = \frac{V_{GS}}{I_G} = \frac{12}{1 \times 10^{-9}} = 12 \times 10^{9}\ \Omega$$

$$\boxed{R_{GS} = 12 \times 10^{3}\ M\Omega.}$$

$\boxed{Q}$ For n-channel silicon FET given half channel height 3×10^{-4} cm. Calculate effective half channel height b given $V_{GS} = V_P/2$.

$\underline{\underline{\text{Soln:}}}$

$$V_{GS} = (1 - b/a)^2\, V_P$$

$$\therefore \frac{1}{2} = (1 - b/a)^2$$

$$b/a = 1 - 0.707$$

$$\boxed{b = 0.878 \times 10^{-4}\ \text{cm.}}$$

$\boxed{Q}$ Pinch-off voltage for n-channel FET given $a = 2 \times 10^{-4}$ cm

$N_D = 125 \times 10^{13}$ cm^{-3}.

$\epsilon = 106.188 \times 10^{-14}$ F/cm.

Soln:

$$V_p = -\frac{q N_D a^2}{2\epsilon}$$

$$V_p = -\frac{1.6\times10^{-19} \times 125\times10^{13} \times 4\times10^{-8}}{2\times106.88\times10^{-14}}$$

$$\therefore \boxed{V_p = -3.74\,V}$$